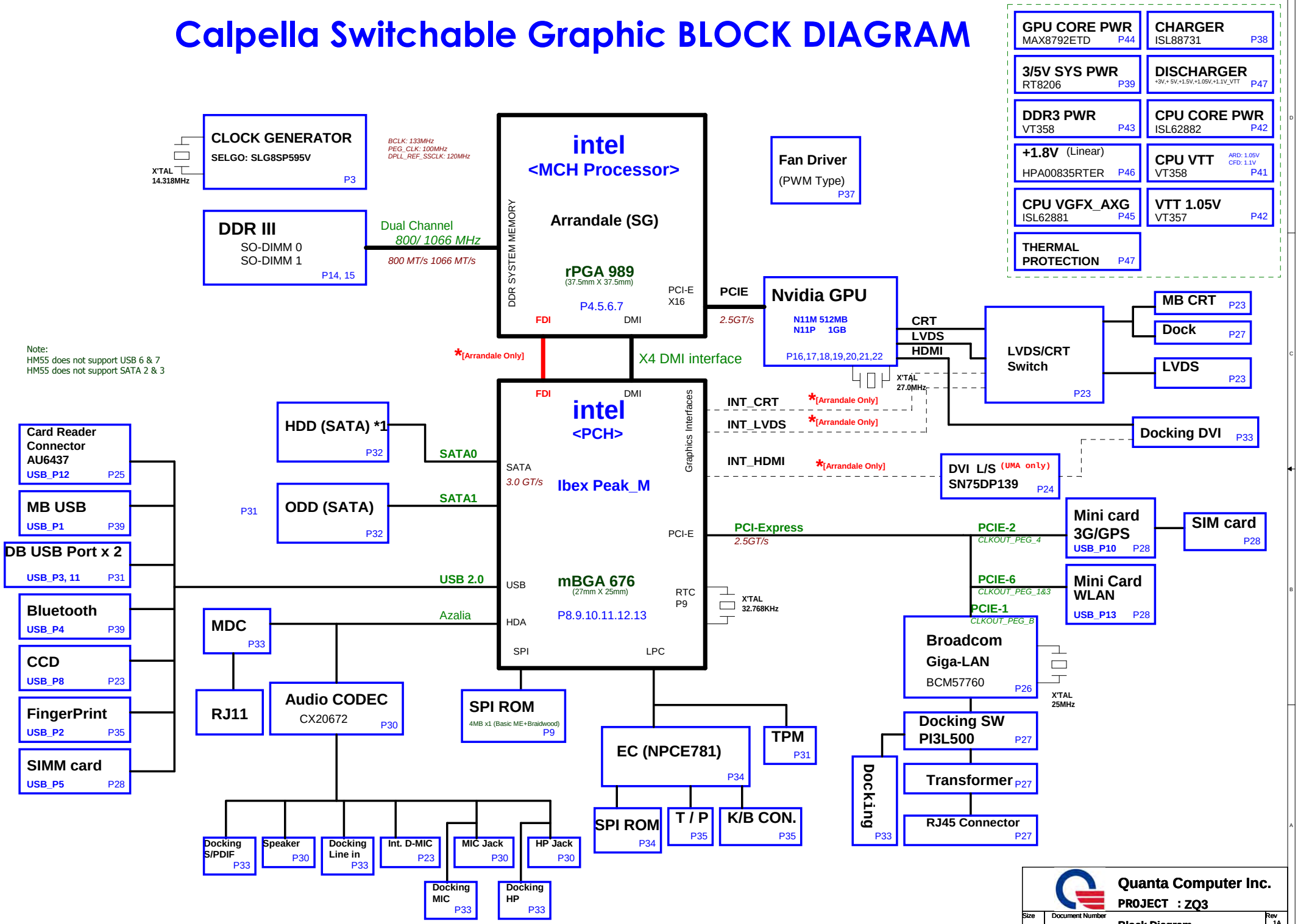
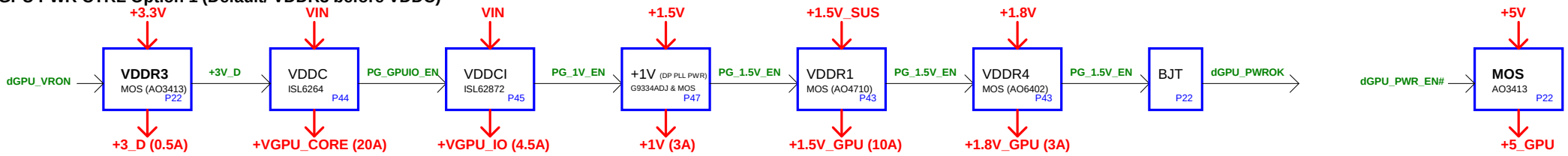
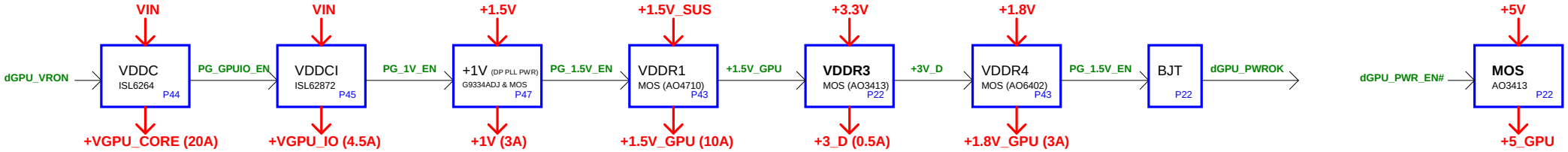
# Calpella Switchable Graphic BLOCK DIAGRAM



## GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



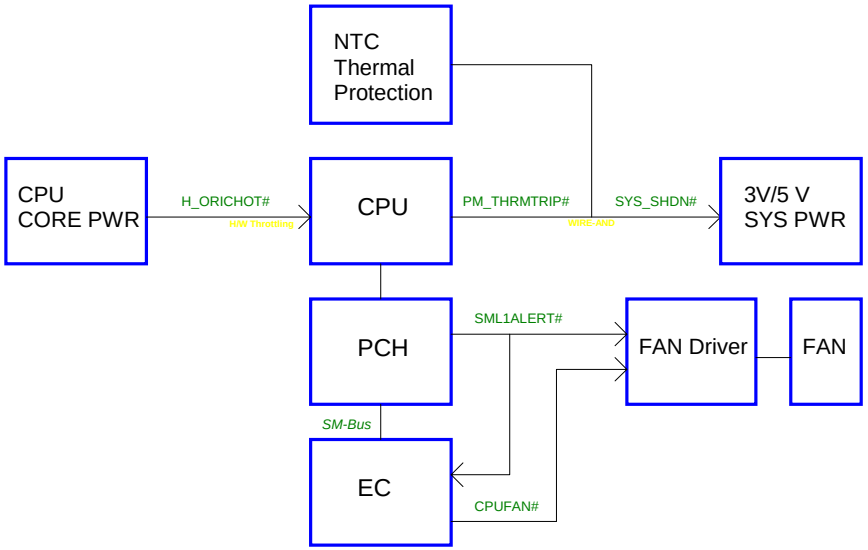

## GPU PWR CTRL Option 2 (VDDR3 after VDDR1)




## Power States

| POWER PLANE | VOLTAGE | DESCRIPTION | CONTROL SIGNAL | ACTIVE IN |
|---|---|---|---|---|
| VIN | +10V~+19V | MAIN POWER | | S0~S5 |
| +RTC_CELL | +3V~+3.3V | RTC | | S0~S5 |
| +3VPCU | +3.3V | 8051 POWER | ALWON | S0~S5 |
| +5VPCU | +5V | CHARGE POWER | ALWON | S0~S5 |
| +15V | +15V | LARGE POWER | +15V_ALWP | S0~S5 |
| 3V_LAN_S5 | +3.3V | LAN POWER | AUX_ON | |
| +5VSUS | +5V | | SUSD | |
| +3VSUS | +3.3V | | SUSD | |
| +1.5VSUS | +1.5V | SODIMM POWER | SUSON | |
| +0.75V_DDR_VTT | +0.9V | SODIMM POWER | MAINON | |
| +5V | +5V | | MAIND | |
| +3V | +3.3V | | MAIND | |
| +1.8V | +1.8V | | MAINON | |
| +1.5V | +1.5V | PCH POWER | MAIND | |
| +1.1V_VTT | +1.05V~+1.1V | CPU POWER | MAINON | |
| +1.05V | +1.05V | PCH POWER | MAINON | |
| +VCC_CORE | 0V~+1.5V | CPU CORE POWER | VRON | |
| LCDVCC | +3.3V | LCD Power | LVDS_VDDEN | |
| MBAT+ | +10V~+17V | MAIN BATTERY | | |
| +5V_S5 | +5V | | S5_ON | |
| +3V_S5 | +3.3V | | S5D | |

## Thermal Follow Chart

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PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | PWR Status & GPU PWR CRL & THRM | 1A |

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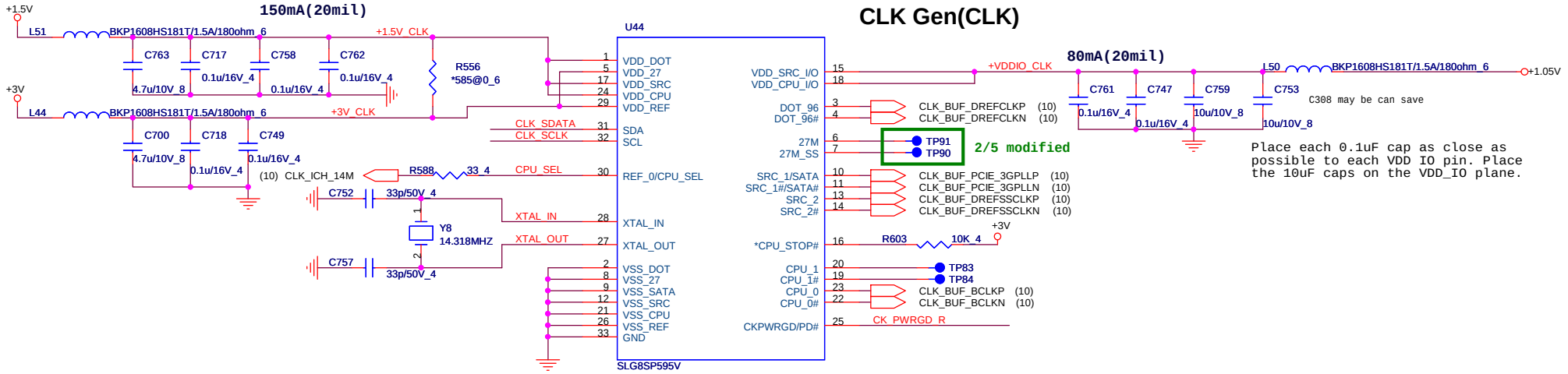
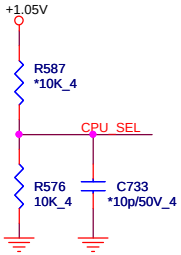
# CLK Gen(CLK)

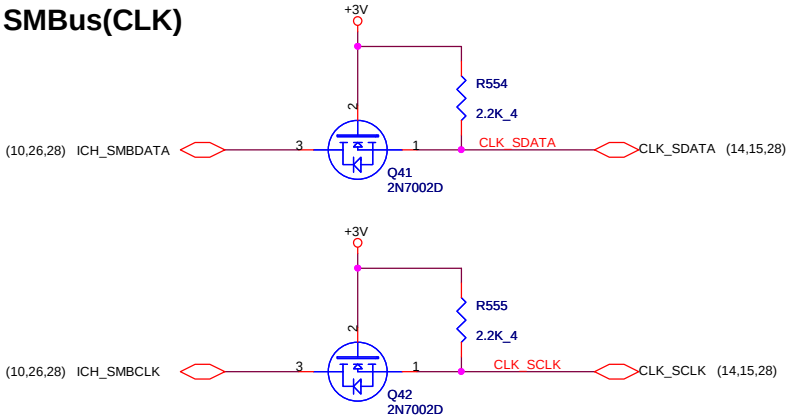



## CPU_CLK select(CLK)

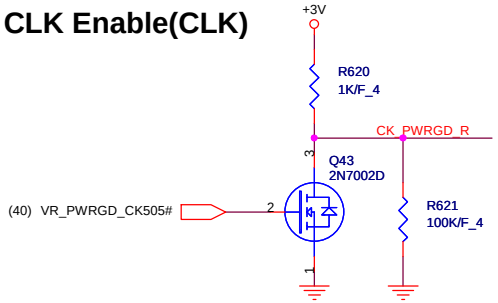



| | 0 | 1 |
|---|---|---|
| CPU_SEL | CPU0/1=133MHz (default) | CPU0/1=100MHz |

## SMBus(CLK)




## CLK Enable(CLK)

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PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | Clock Generator | 1A |

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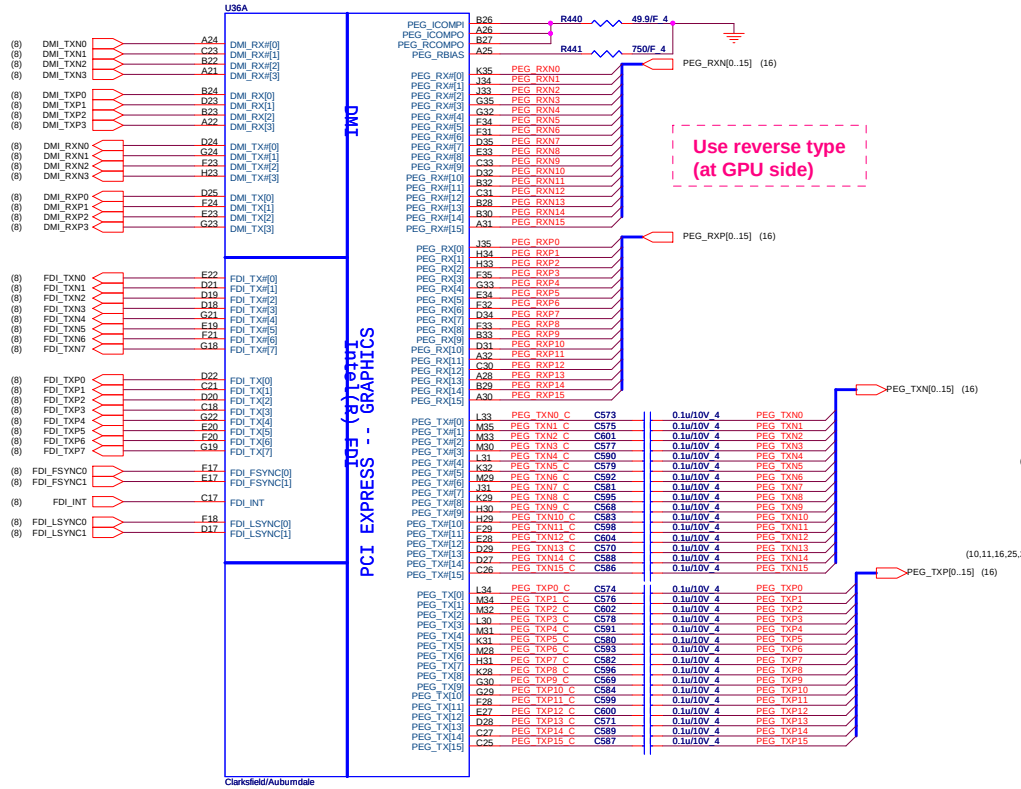
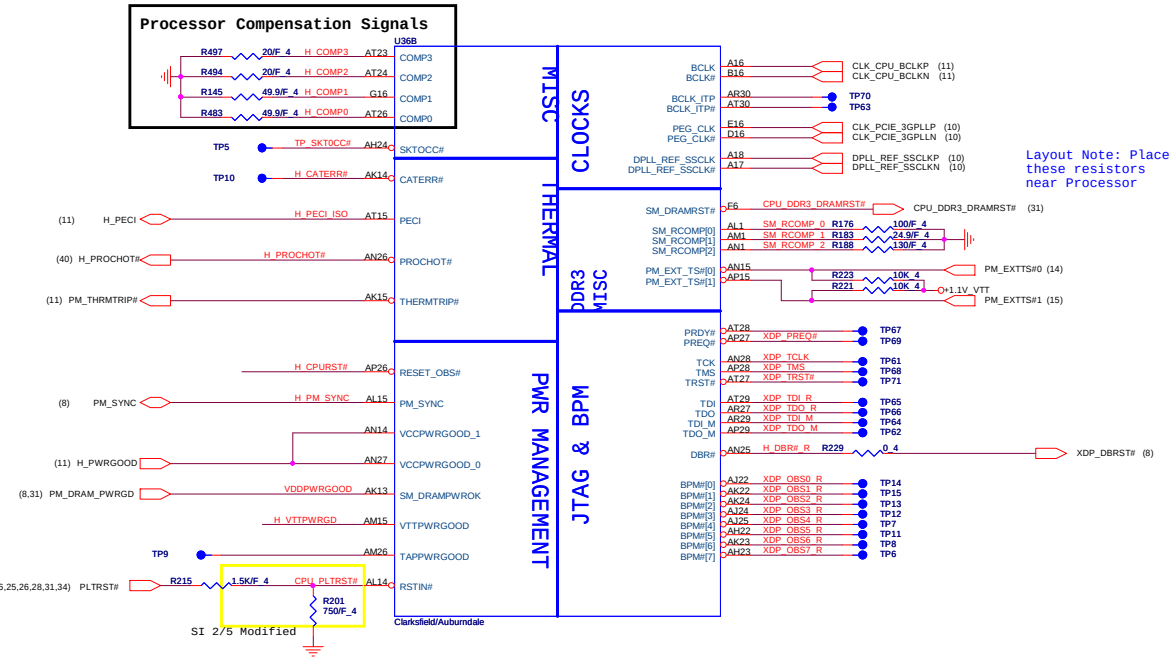
Arrandale_1(CPU)

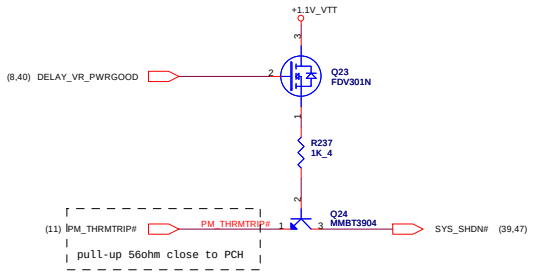
# AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



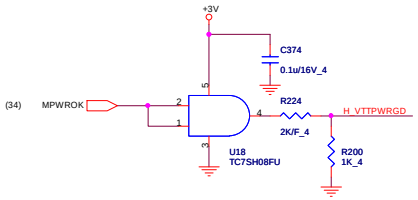

# AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



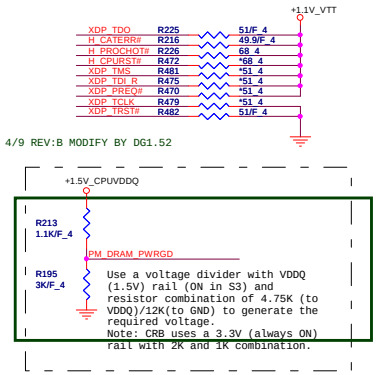

## Thermaltrip protect



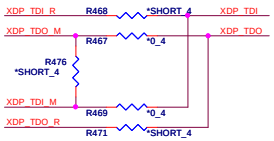

## VTT PWR_Good




## Processor pull-up




## JTAG MAPPING



| | |
|---|---|
| Scan Chain (Default) | STUFF -> R469, R491, R507<br>NO STUFF -> R489, R490 |
| CPU Only | STUFF -> R490, R491<br>NO STUFF -> R469, R489, R507 |
| GMCH Only | STUFF -> R489, R507<br>NO STUFF -> R491, R490, R469 |

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|---|---|---|
| | AUBURNDA 1/4 | 1A |

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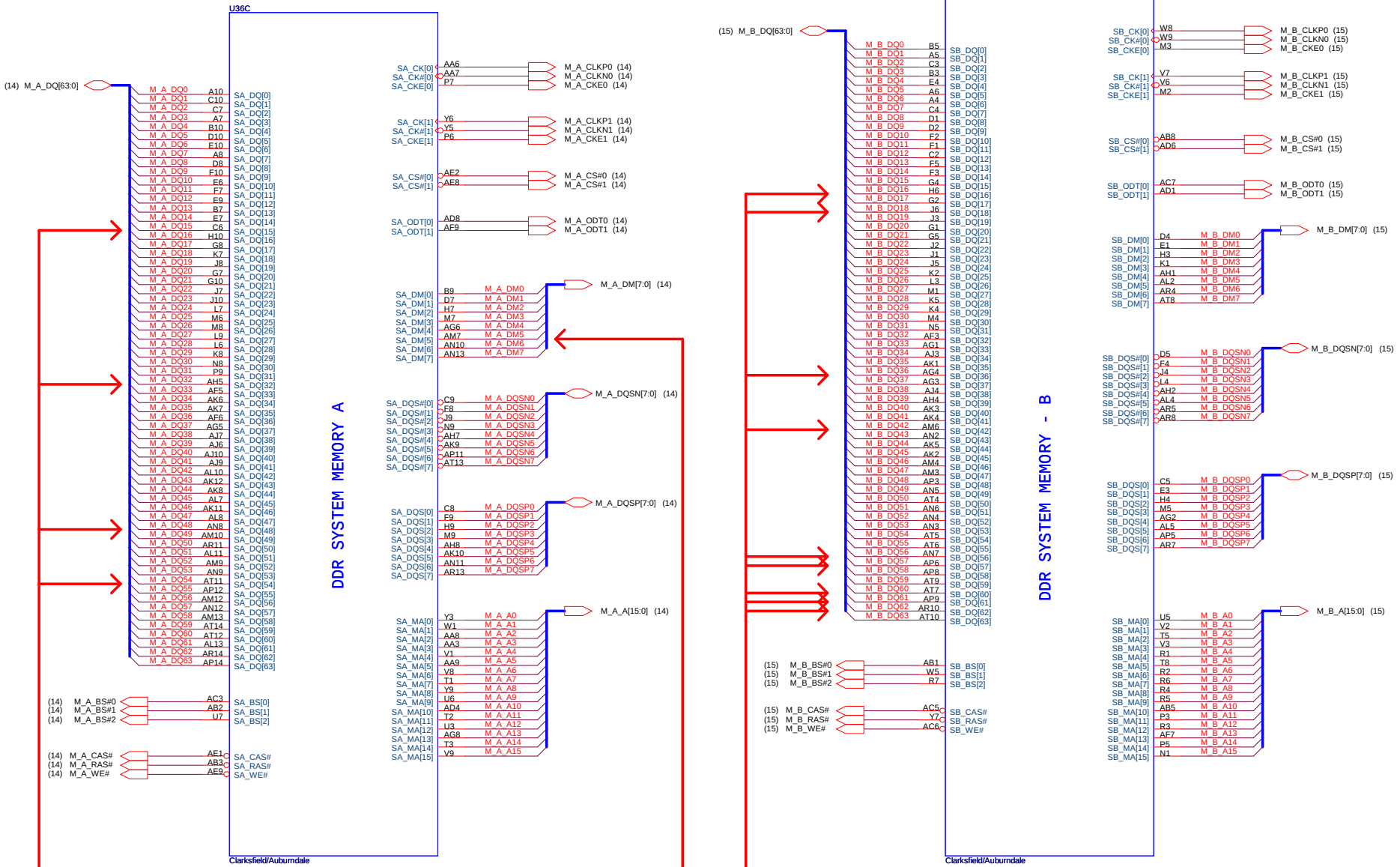
# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

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|---|---|---|
| | AUBURNDA 2/4 | 1A |

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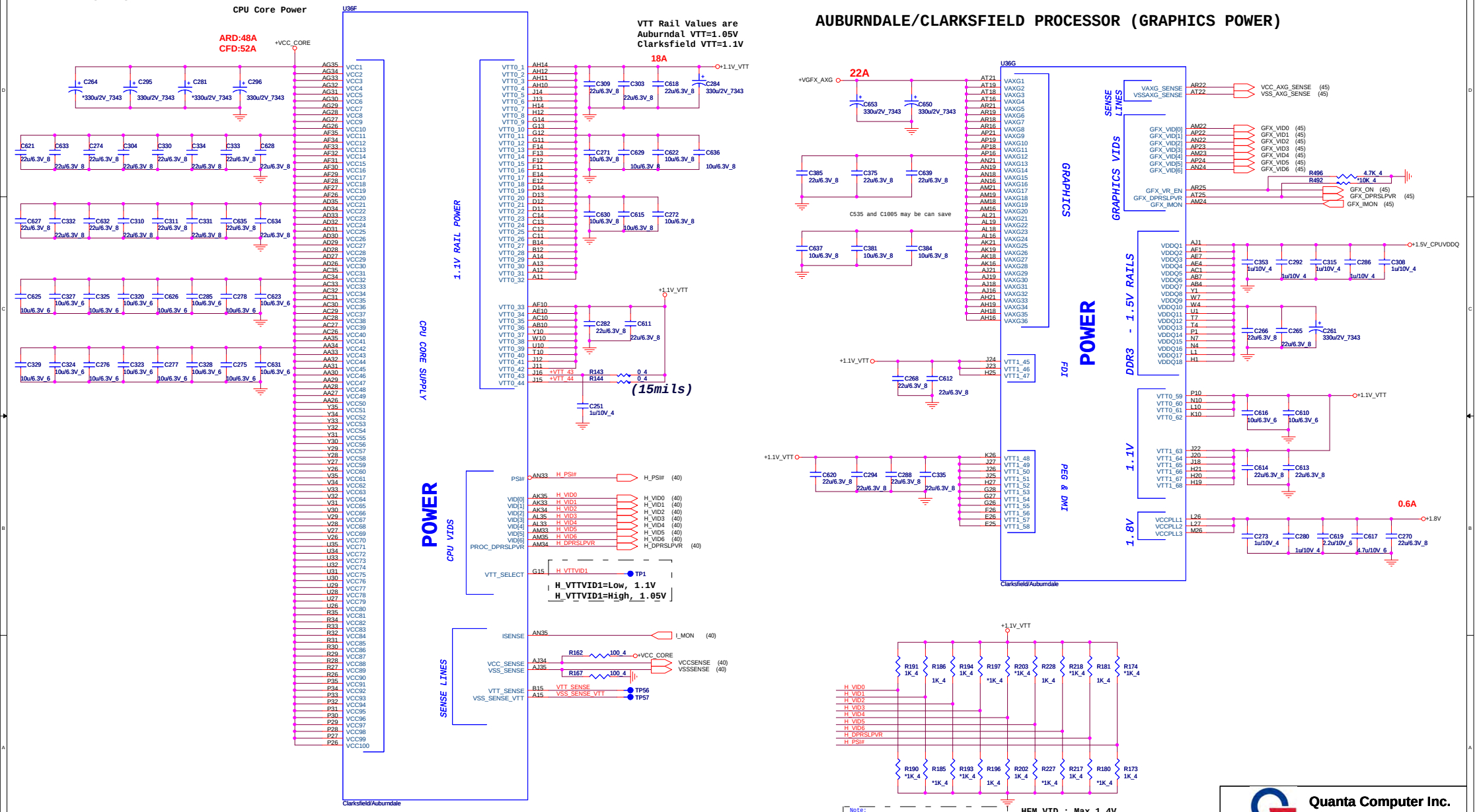
# Arrandale_3(CPU)

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PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | AUBURNDA 3/4 (PWR) | 1A |

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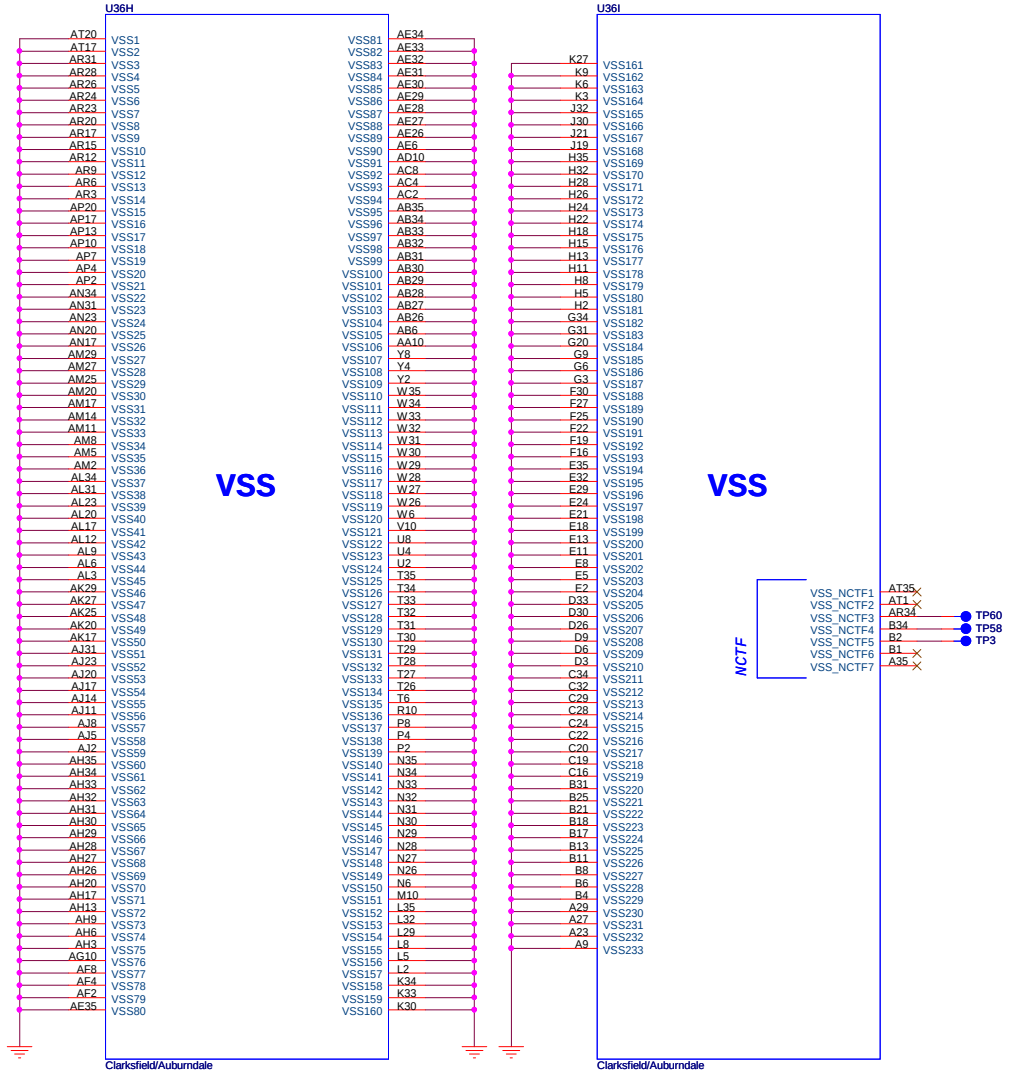
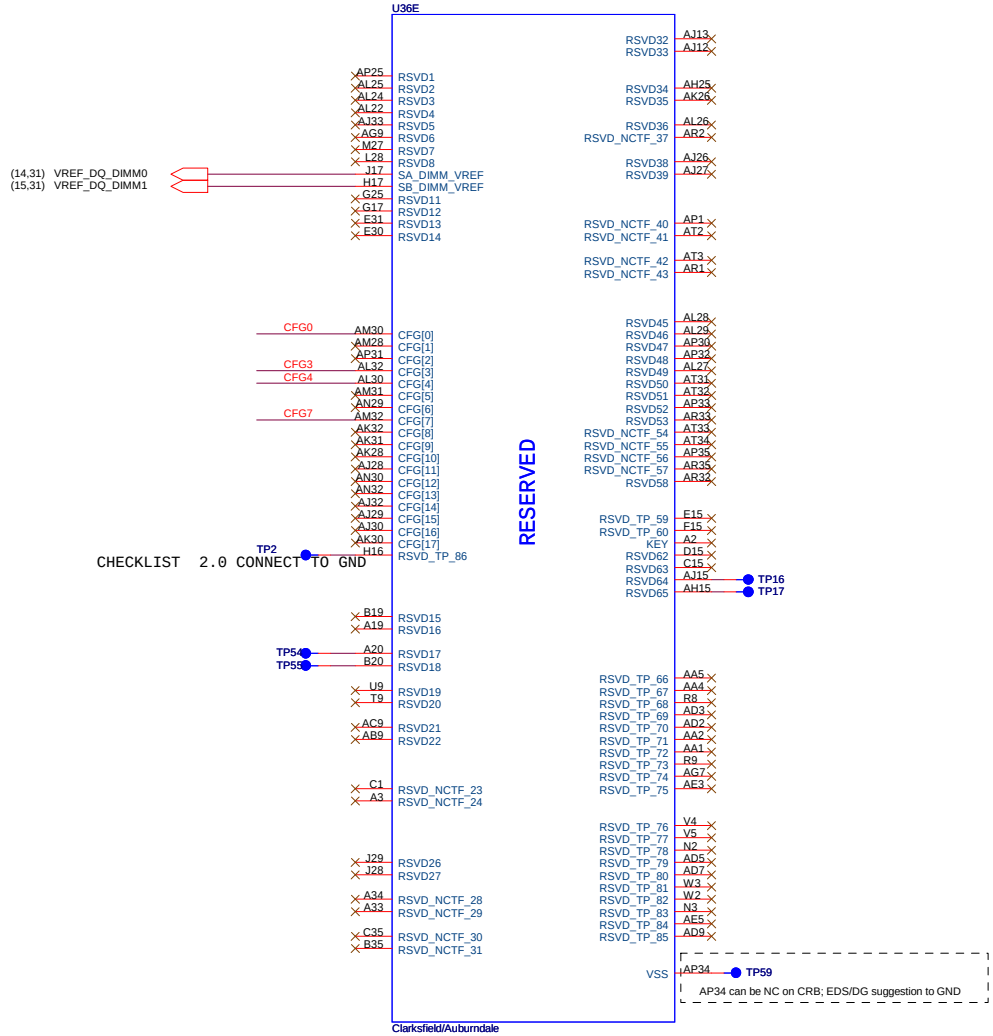
# Arrandale_4(CPU)

## AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

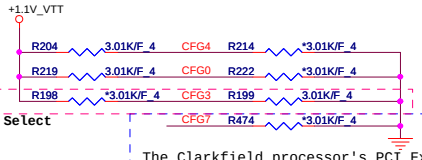



## AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)




## Processor Strapping

| | 1 | 0 |
|---|---|---|
| CFG4 (Display Port Presence) | Disabled; No Physical Display Port attached to Embedded Diplay Port | Enabled; An external Display port device is connected to the Embedded Display port |
| CFG0 (PCI-Epress Configuration Select) | Single PEG | Bifurcation enabled |
| CFG3 (PCI-Epress Static Lane Reversal) | Normal Operation | Lane Numbers Reversed |




**CFG[ 1:0 ] - PCI_Epress Configuration Select**
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

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|---|---|---|
| | AUBURNDA 4/4 | 1A |

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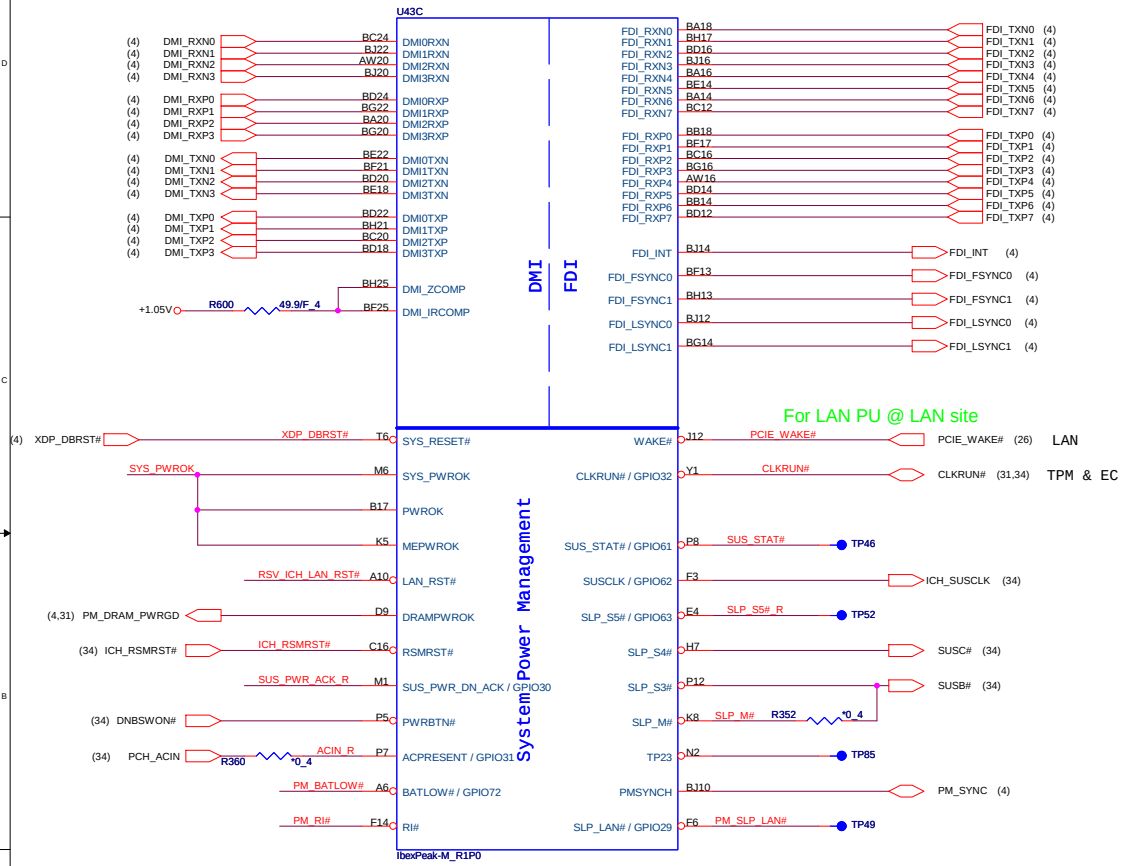
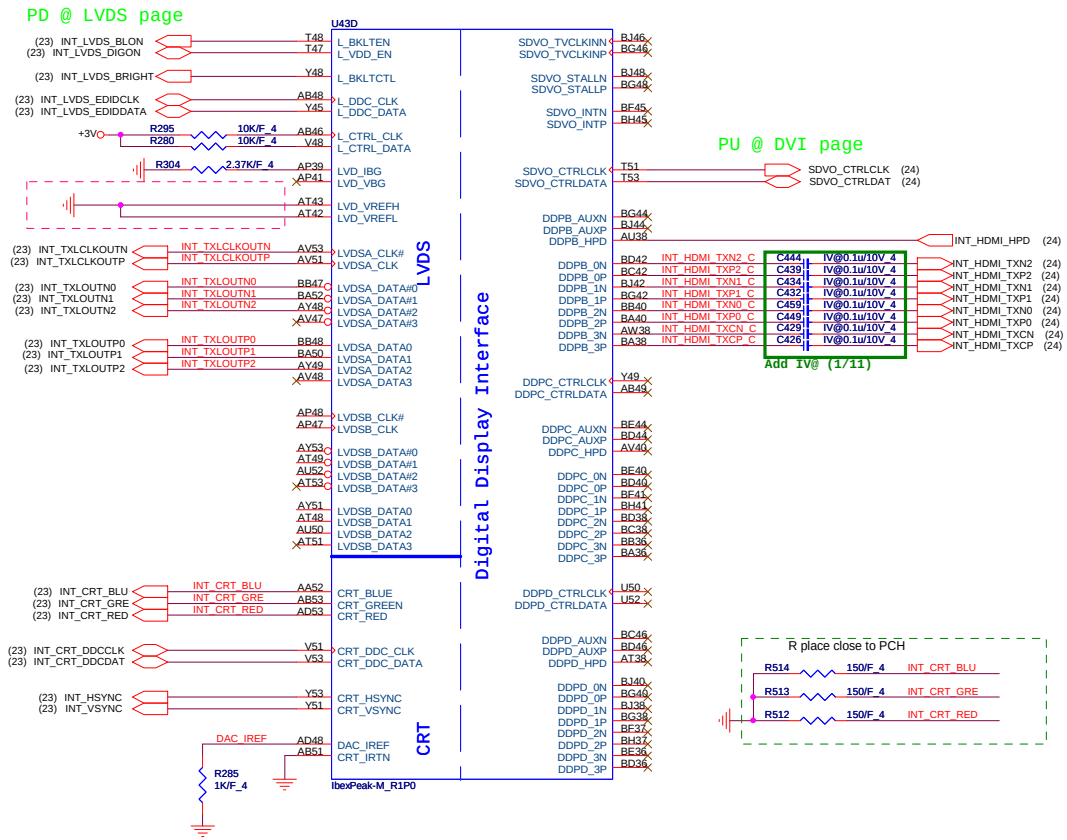
# PCH1(CLG)

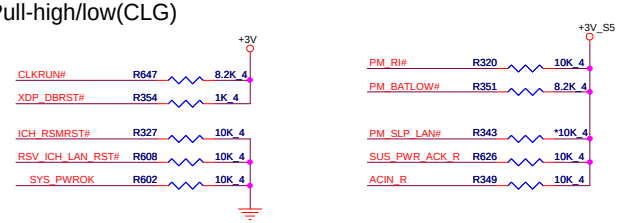
## IBEX PEAK-M (DMI,FDI,GPIO)



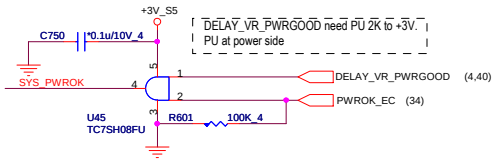

## IBEX PEAK-M (LVDS,DDI)




## PCH Pull-high/low(CLG)




## System PWR_OK(CLG)




Quanta Computer Inc.

PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | IBEX PEAK-M 1/6 | 1A |

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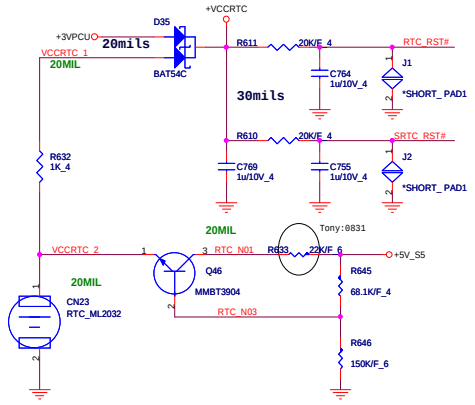
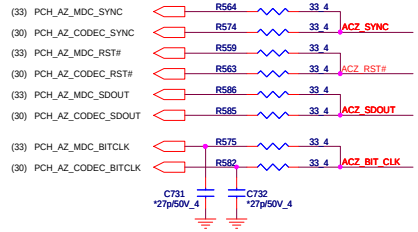
## RTC Circuitry(RTC)



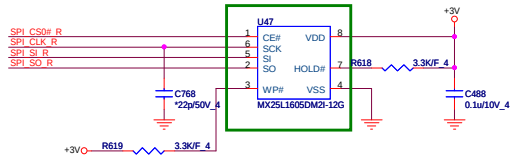

## HDA Bus(CLG)




Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

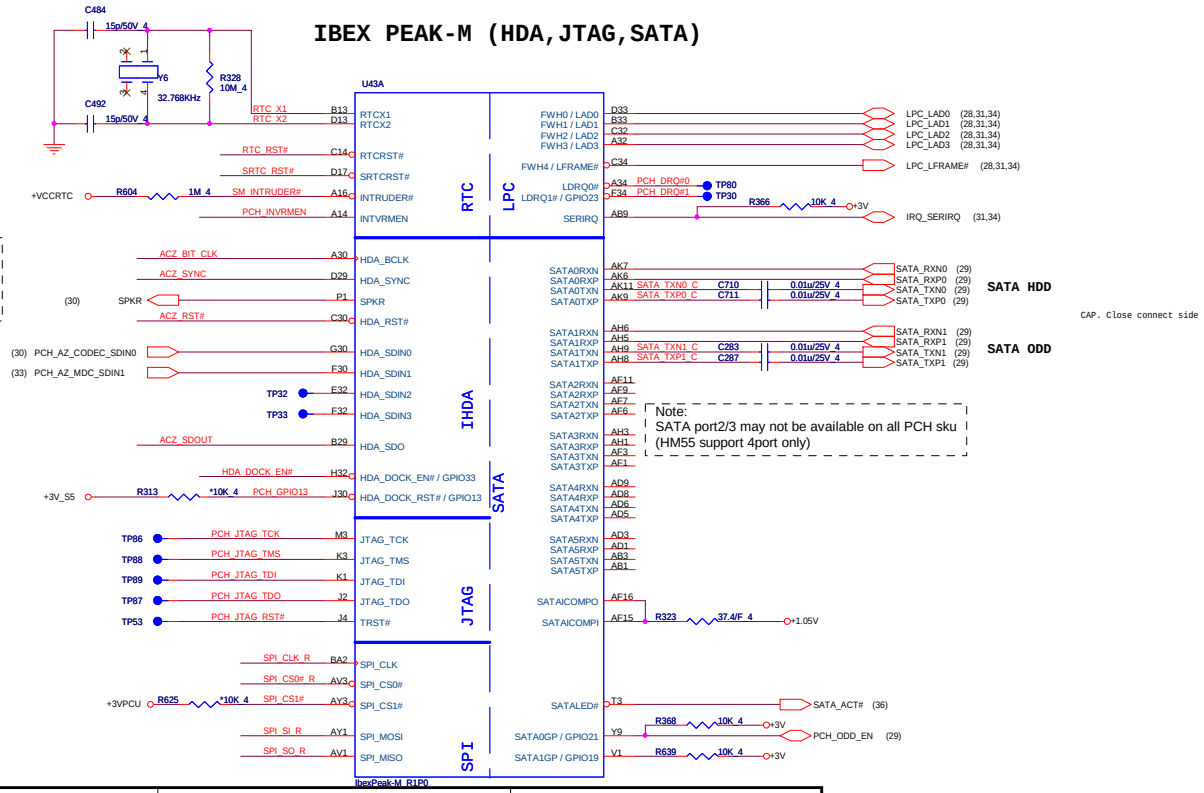
## PCH SPI(CLG)

2/10 modify for fac. request.




## PCH2(CLG)

### IBEX PEAK-M (HDA,JTAG,SATA)



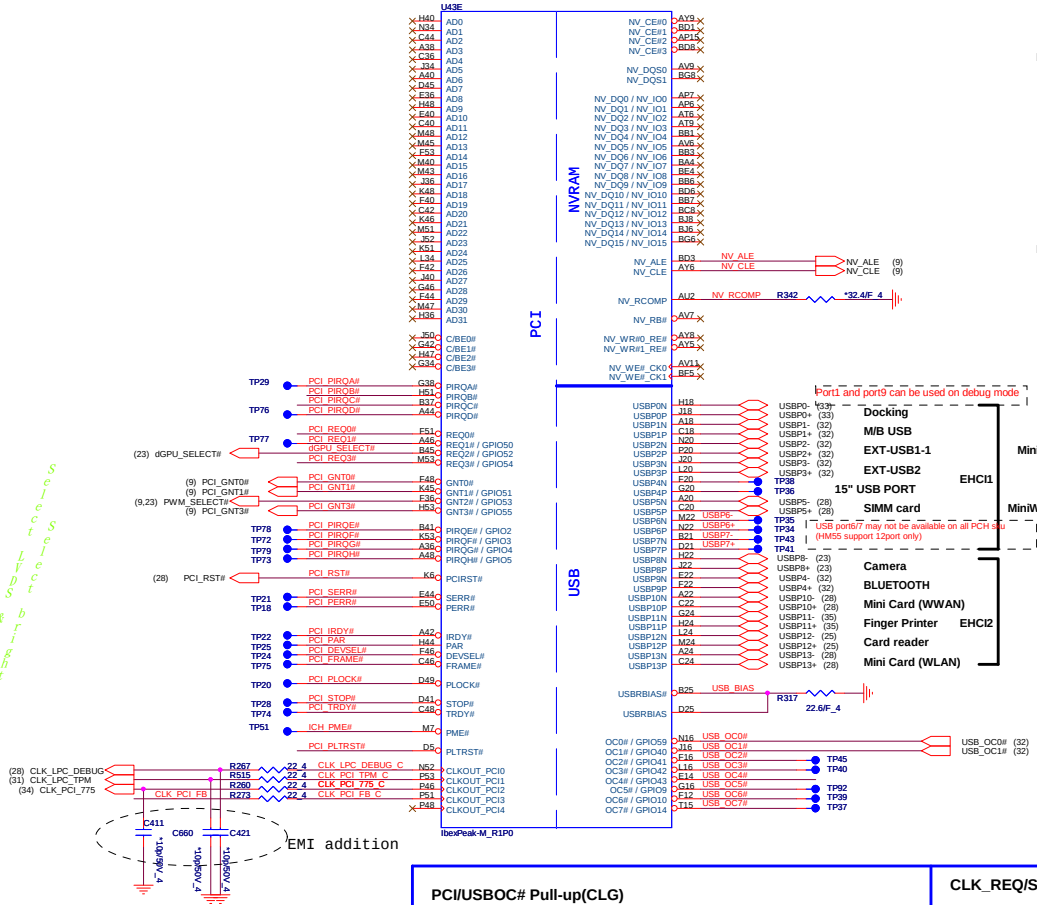

## PCH Strap Table

| Pin Name | Strap description | Sampled | Configuration | ZY9B note |
|---|---|---|---|---|
| SPKR | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode | +3V R642 *10K_4 SPKR |
| INIT3_3V | Reserved | PWROK | 1 = Default (weak pull-up 20K)<br>Should not be pull-down | |
| GNT3# / GPIO55 | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K) | R519 *4.7K_4 PCI_GNT3# (10) |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up | +VCCRTC R606 330K_4 PCH_INVRMEN |
| GNT1# / GPIO51 | Boot BIOS Selection 1 [bit-1] | PWROK | GNT1# / GNT0# / Boot Location<br>1 / 1 / SPI<br>1 / 0 / PCI<br>0 / 0 / LPC | Default weak pull-up on GNT0/1#<br>[Need external pull-down for LPC BIOS]<br>+3V R284 *1K_4 R269 *1K_4 R292 1K_4 R268 1K_4 1/11 modified<br>PCI_GNT0# (10)<br>PCI_GNT1# (10) |
| GNT0# | Boot BIOS Selection 0 [bit-0] | PWROK | | |
| GNT2# / GPIO53 | ESI strap (Server only) | PWROK | Should not be pull-down<br>(weak pull-up 20K) | R303 *4.7K_4 PWM_SELECT# (10,23) |
| NV_ALE | Intel Anti-Theft HDD protection | PWROK | 0 = Disable (Internal pull-down 32ohm) | +1.8V R624 *1K_4 NV_ALE NV_ALE (10) |
| NV_CLE | DMI Termination voltage | PWROK | weak pull-down 32ohm | +1.8V R341 *1K_4 NV_CLE NV_CLE (10) |
| HDA_DOCK_EN#/GPIO33 | Flash Descriptor Security | PWROK | 0 = Override<br>1 = Default (weak pull-up 20K) | +3V R592 *1K_4 R594 *10K_4 HDA_DOCK_EN# |
| SPI_MOSI | iTPM function Disable | MEPWROK | 0 = Default (weak pull-down 20K)<br>1 = Enable | +3V R623 *8.2K_4 SPI_SI_R |
| HDA_SDO | Reserved | RSMRST# | Should not be pull-up<br>(weak pull-down 20K) | |
| GPIO8 | Reserved | RSMRST# | Should not be pull-down<br>(weak pull-up 20K) | +3V_S5 R336 10K_4 RSV_GPIO8 (11) |
| GPIO27 | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable<br>1 = Enable (weak pull-up 20K) | R324 *10K_4 RSV_GPIO27 (11) |
| HDA_SYNC | On-die PLL PWR supply select | RSMRST# | 0 = 1.8V supply (weak pull-down 20K)<br>1 = 1.5V supply | use defaul (0 = 1.8V supply) |
| GPIO15 | Reserved | RSMRST# | 0 = TLS no Confidentiality<br>(weak pull-down 20K)<br>1 = TLS Confidentiality | +3V_S5 R346 1K_4 CR_WAKE# (11) |

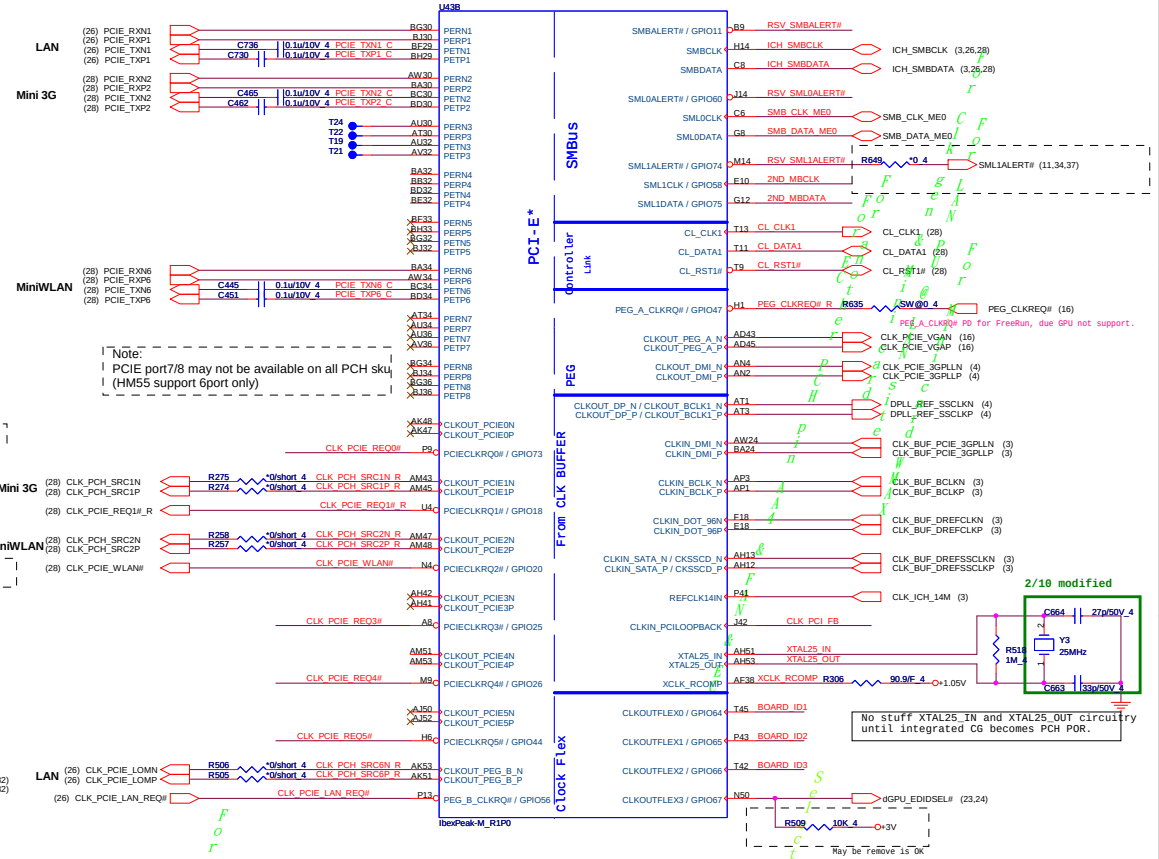
from PCH and to control SW (EC or PCH control Brightness switch)

# PCH3(CLG)

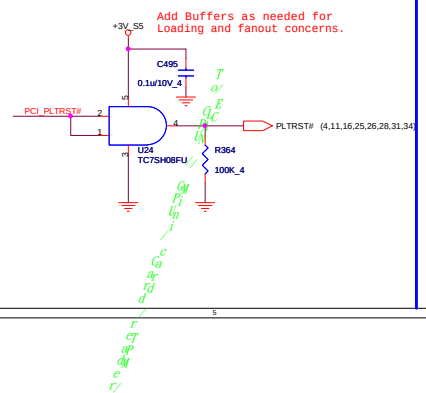
## IBEX PEAK-M (PCI,USB,NVRAM)



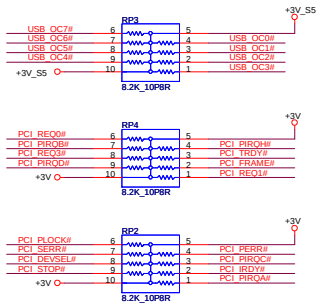

## IBEX PEAK-M (PCI-E,SMBUS,CLK)



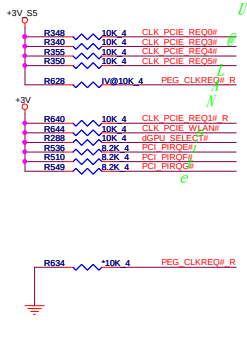

## PLTRST#(CLG)




## PCI/USBOC# Pull-up(CLG)



## CLK_REQ/Strap Pin(CLG)



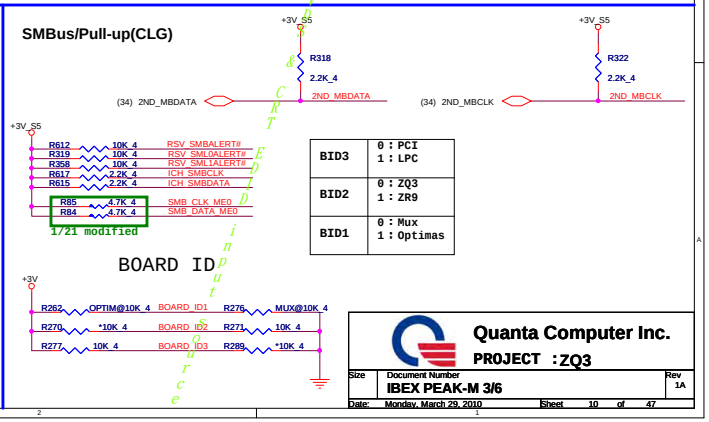
| A16 swap override Strap/Top-Block Swap Override jumper | |
|---|---|
| PCI_GNT3# | Low = A16 swap override/Top-Block Swap Override enabled<br>High = Default |

| Boot BIOS Strap | | |
|---|---|---|
| GNT0# | GNT1# | Boot BIOS Location |
| 0 | 0 | LPC |
| 0 | 1 | Reserved (NAND) |
| 1 | 0 | PCI |
| 1 | 1 | SPI |

| Danbury Technology Enabled | |
|---|---|
| NV_ALE | High = Enable<br>Low = Disable |

| DMI Termination Voltage | |
|---|---|
| NV_CLE | Set to Vcc when LOW<br>Set to Vcc/2 when HIGH |

## SMBus/Pull-up(CLG)



| BID3 | 0 : PCI<br>1 : LPC |
|---|---|
| BID2 | 0 : ZQ3<br>1 : ZR9 |
| BID1 | 0 : Mux<br>1 : Optimas |

BOARD ID

Quanta Computer Inc.

PROJECT :ZQ3

Size | Document Number: IBEX PEAK-M 3/6 | Rev 1A

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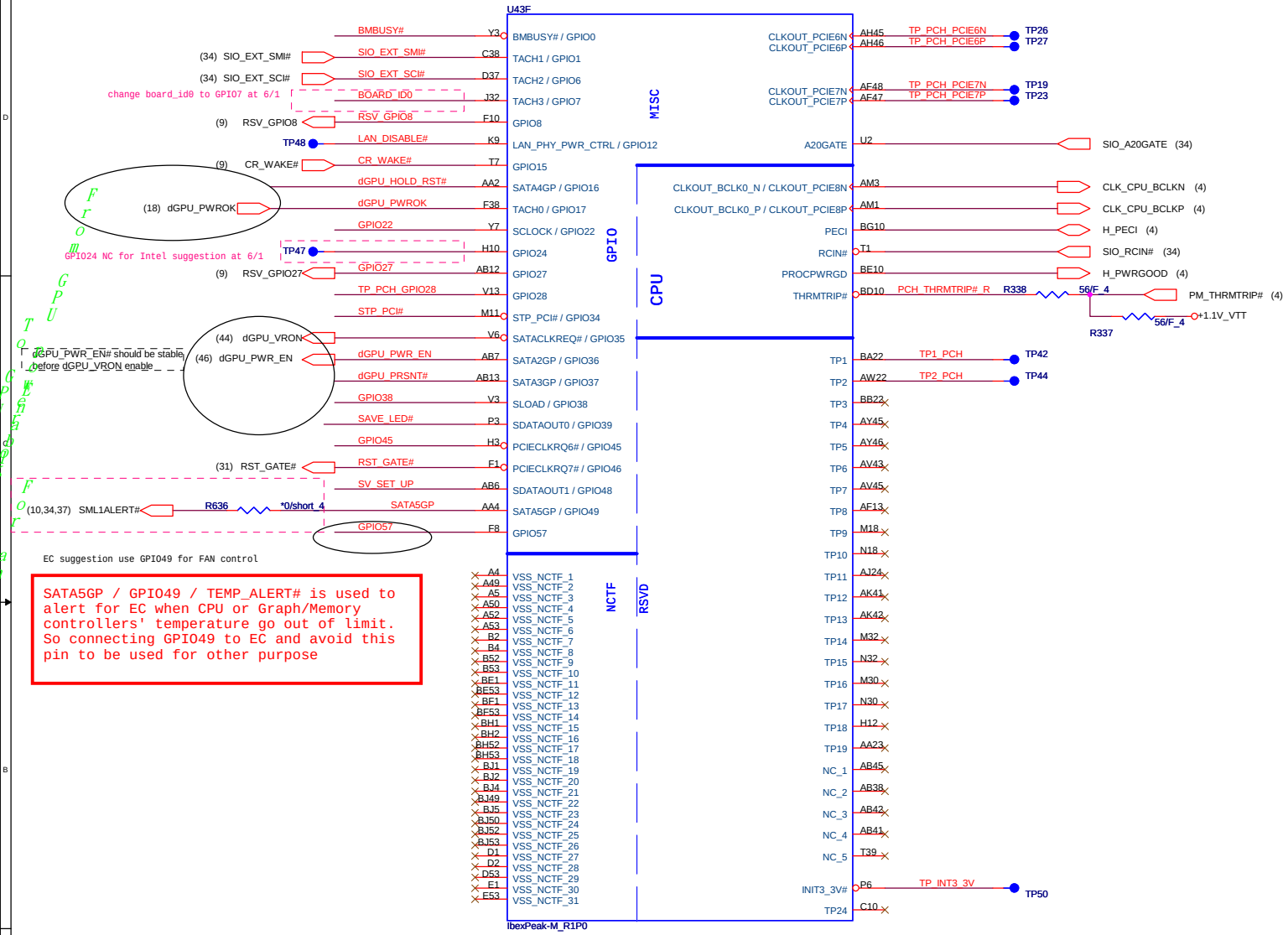
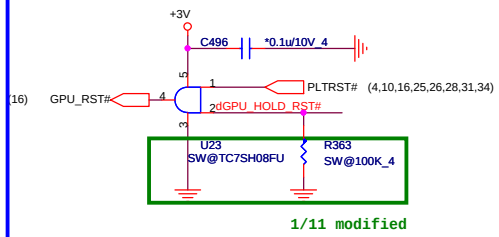
# PCH4(CLG)

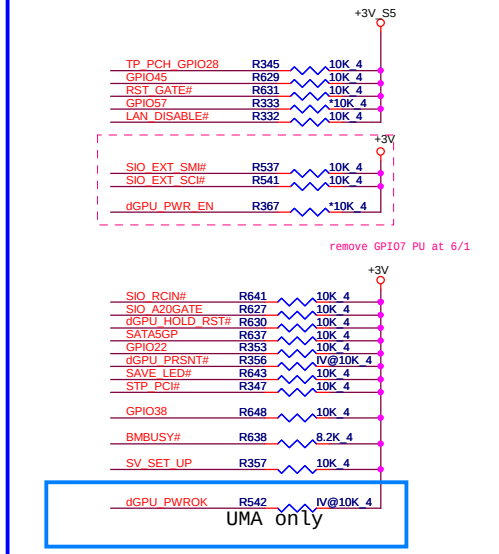
# IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



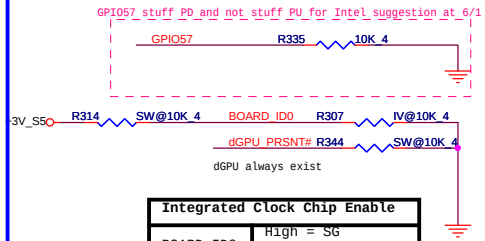

## GPU RST#(CLG)




## GPIO Pull-up/Pull-down(CLG)




| | |
|---|---|
| SV_SET_UP | 1-X High = Strong (Default) |




| Integrated Clock Chip Enable | |
|---|---|
| BOARD_ID0 | High = SG<br>Low = UMA |
| RSV_GPIO8 | High = Disable<br>Low = Enable |

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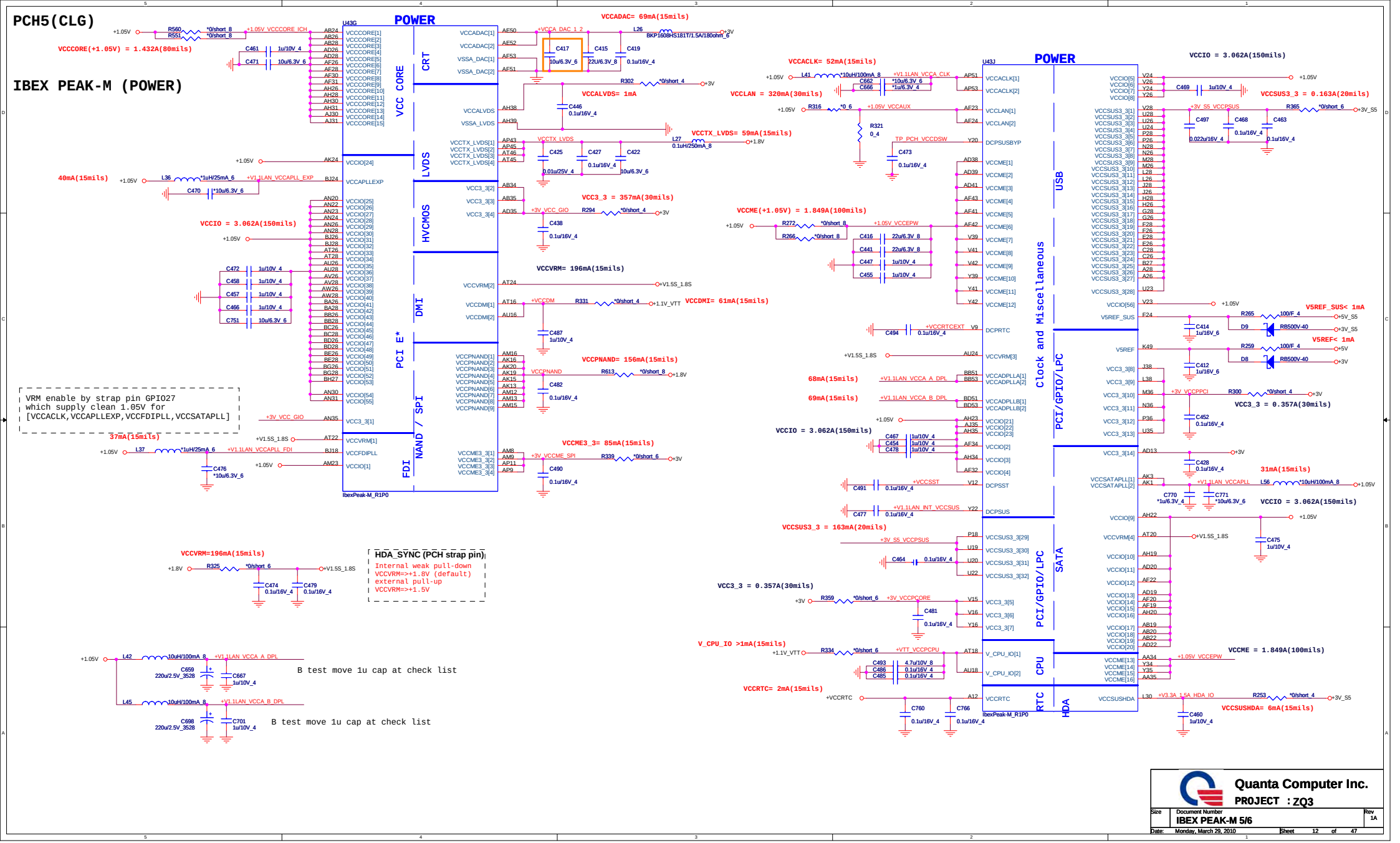
PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | IBEX PEAK-M 4/6 | 1A |

Date: Monday, March 29, 2010 Sheet 11 of 47

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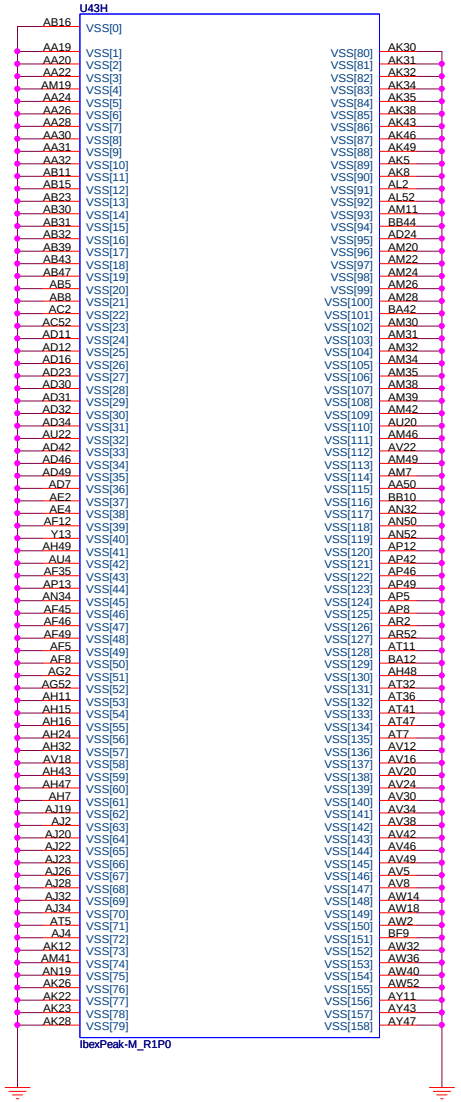
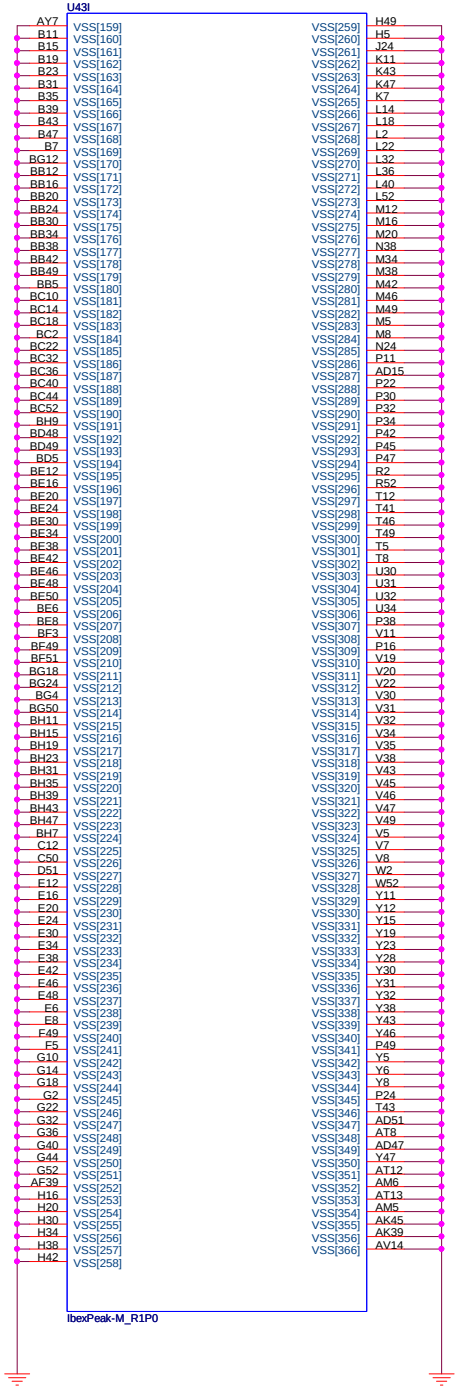
# PCH6(CLG)

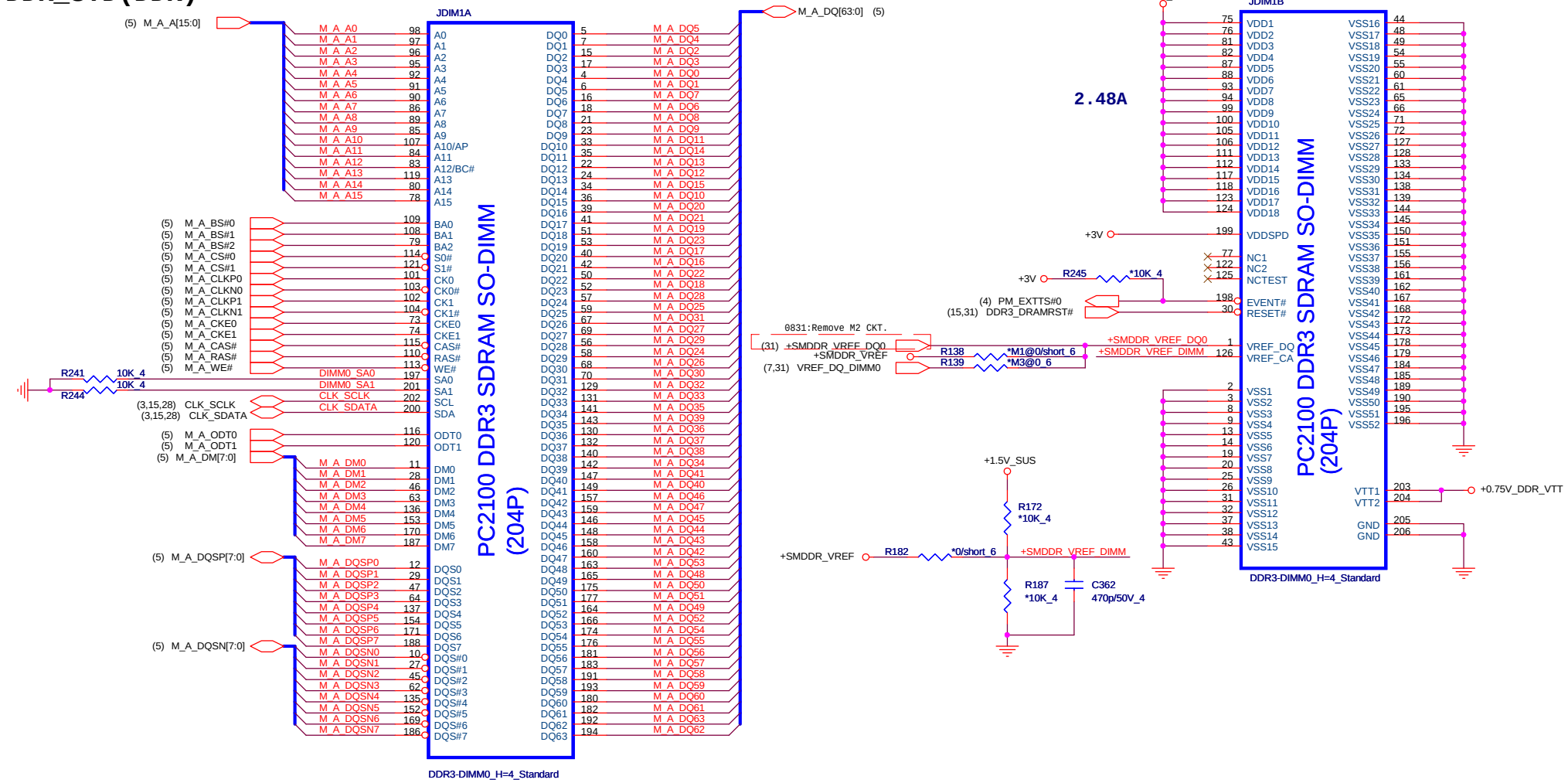
## IBEX PEAK-M (GND)



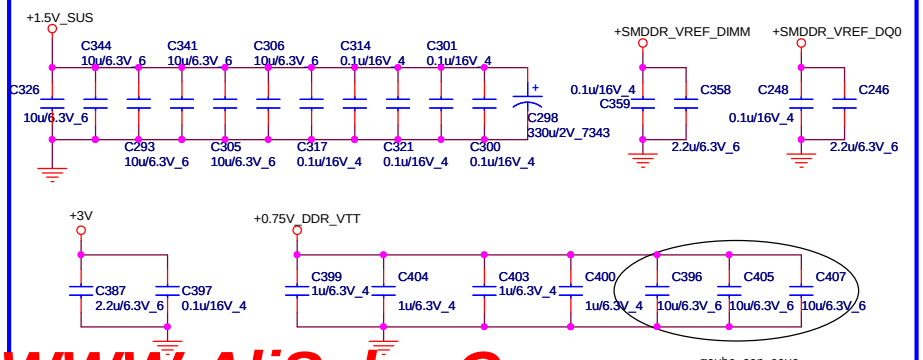




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZQ3 | | |
| Size | Document Number: IBEX PEAK-M 6/6 | Rev 1A |
| Date: Monday, March 29, 2010 | Sheet 13 of 47 | |

# DDR_STD(DDR)




## Place these Caps near So-Dimm0.

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PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | DDRIII SO-DIMM-0 | 1A |

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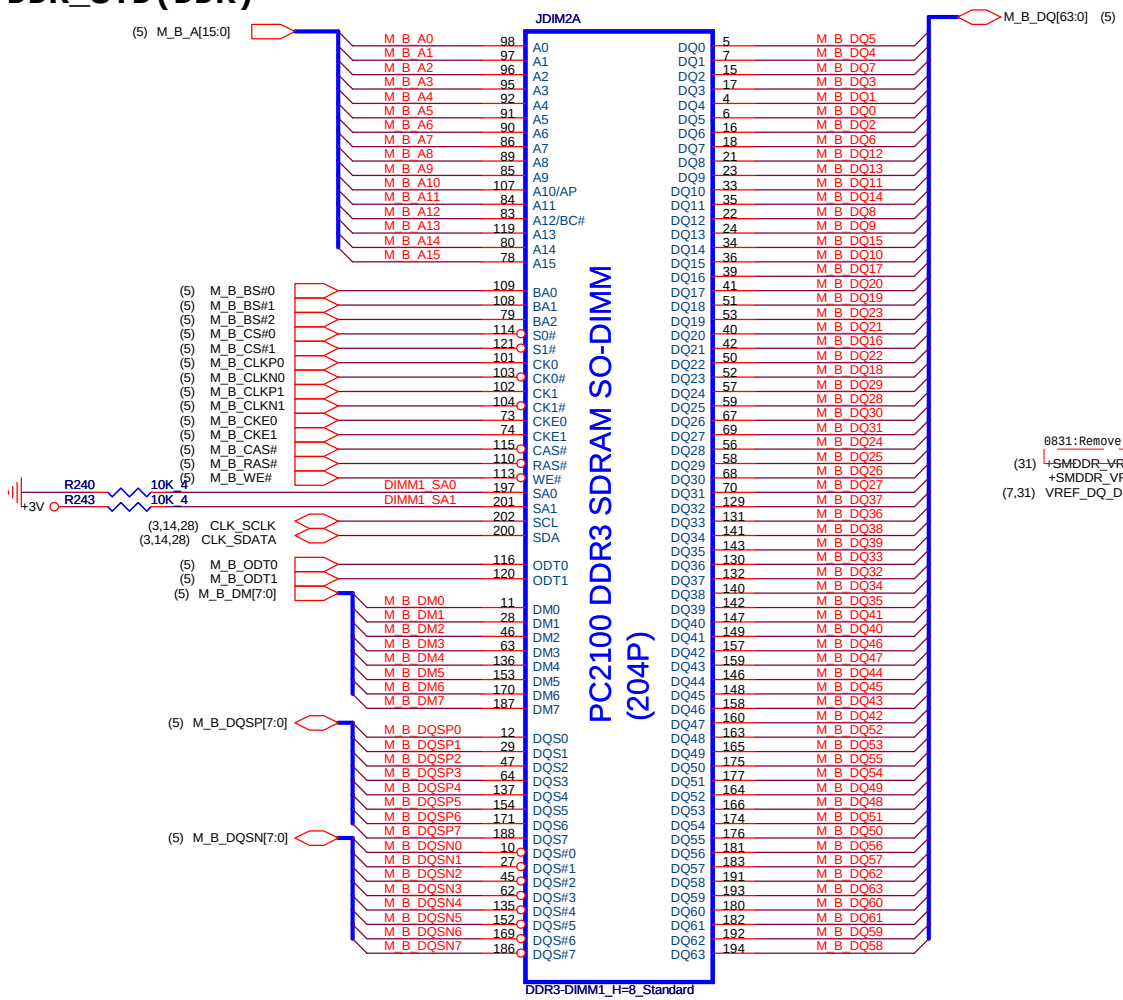
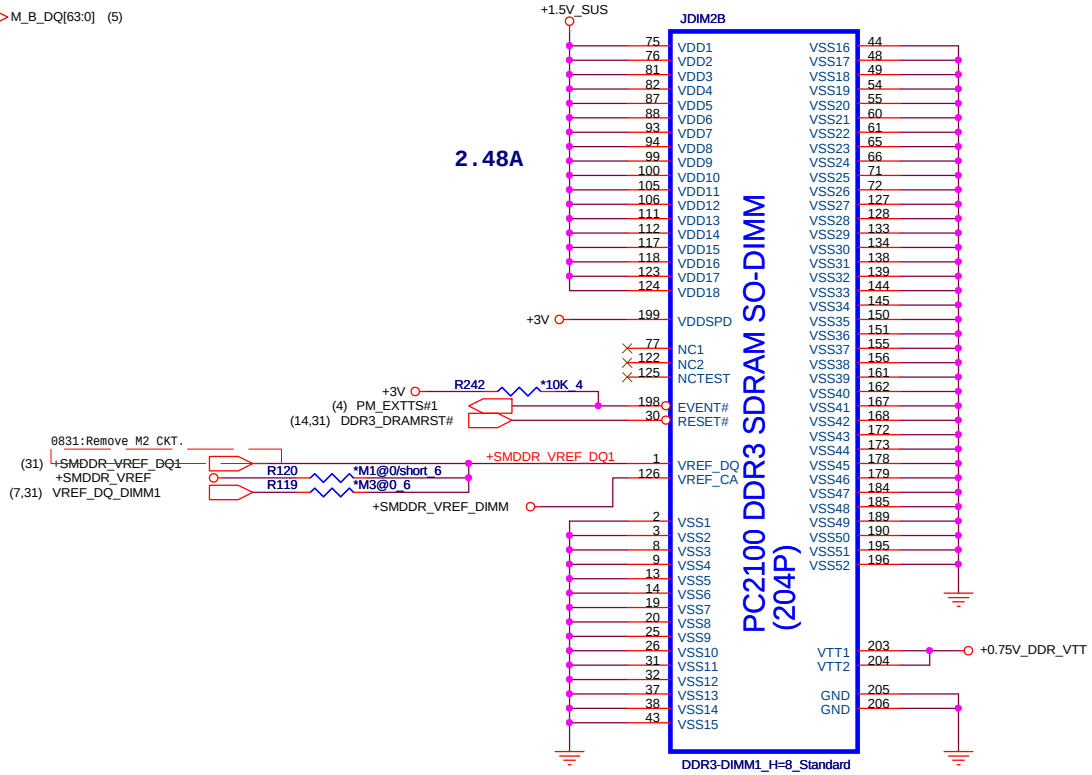
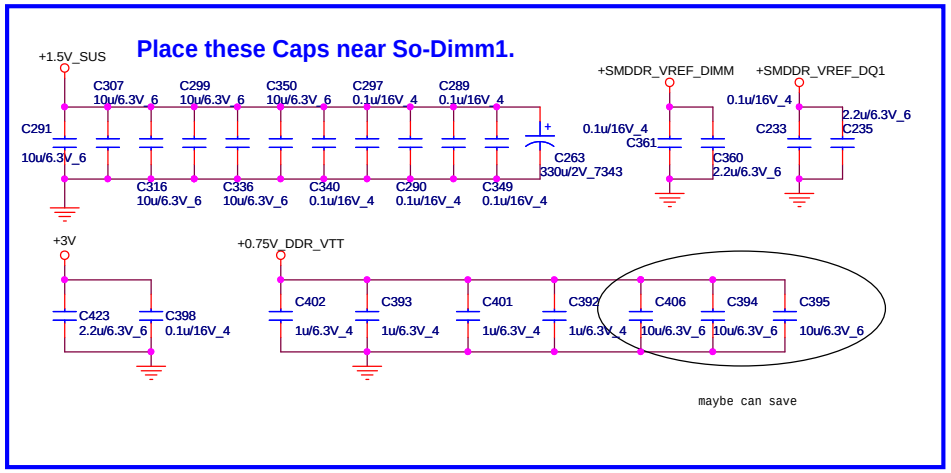
# DDR_STD(DDR)




Quanta Computer Inc.

PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | DDRIII SO-DIMM-1 | 1A |
| Date: Monday, March 29, 2010 | Sheet 15 of 47 | |

# GPU_1(VGA)

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

N11P GPU : AJ0N11P0T05
N11M GPU : AJ0N11M0T07

N11P_A2 GPU : AJ0N11P0T20
N11M_B1 GPU : AJ0N11M0T22

~ 500mA

1600mA

Near BGA

12~16 mils width 110mA

10/20 add

10/20 del C3553,C3554

12~16 mils width

10/20 Modify to 1uF

U32A COMMON

PCI EXPRESS

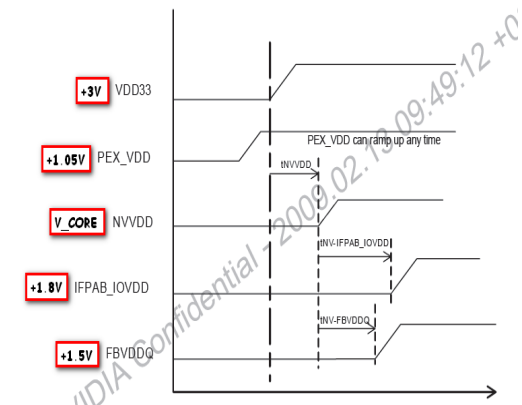
CSP@N11P-GE1-A3

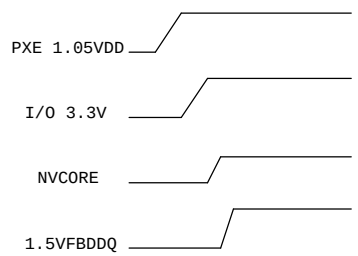
1211 for Nvidia request add transition cap

R450 un-mount for switchable function

Only for Hybrid

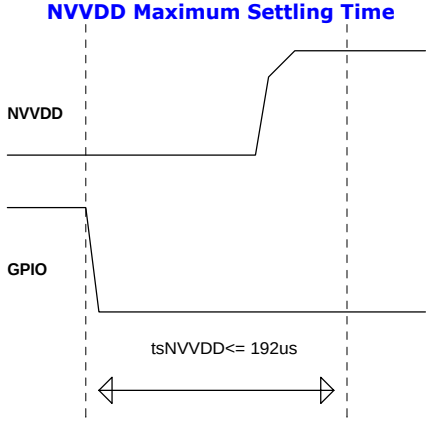
## power up sequence



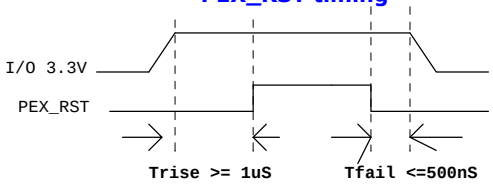




NB9M: VGACORE +0.90V (Normal) , +1.09V

### NVVDD Maximum Settling Time




### PEX_RST timing




Quanta Computer Inc.
PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | N11P-GE (PCIE I/F) 1/5 | 1A |

Date: Monday, March 29, 2010 Sheet 16 of 47

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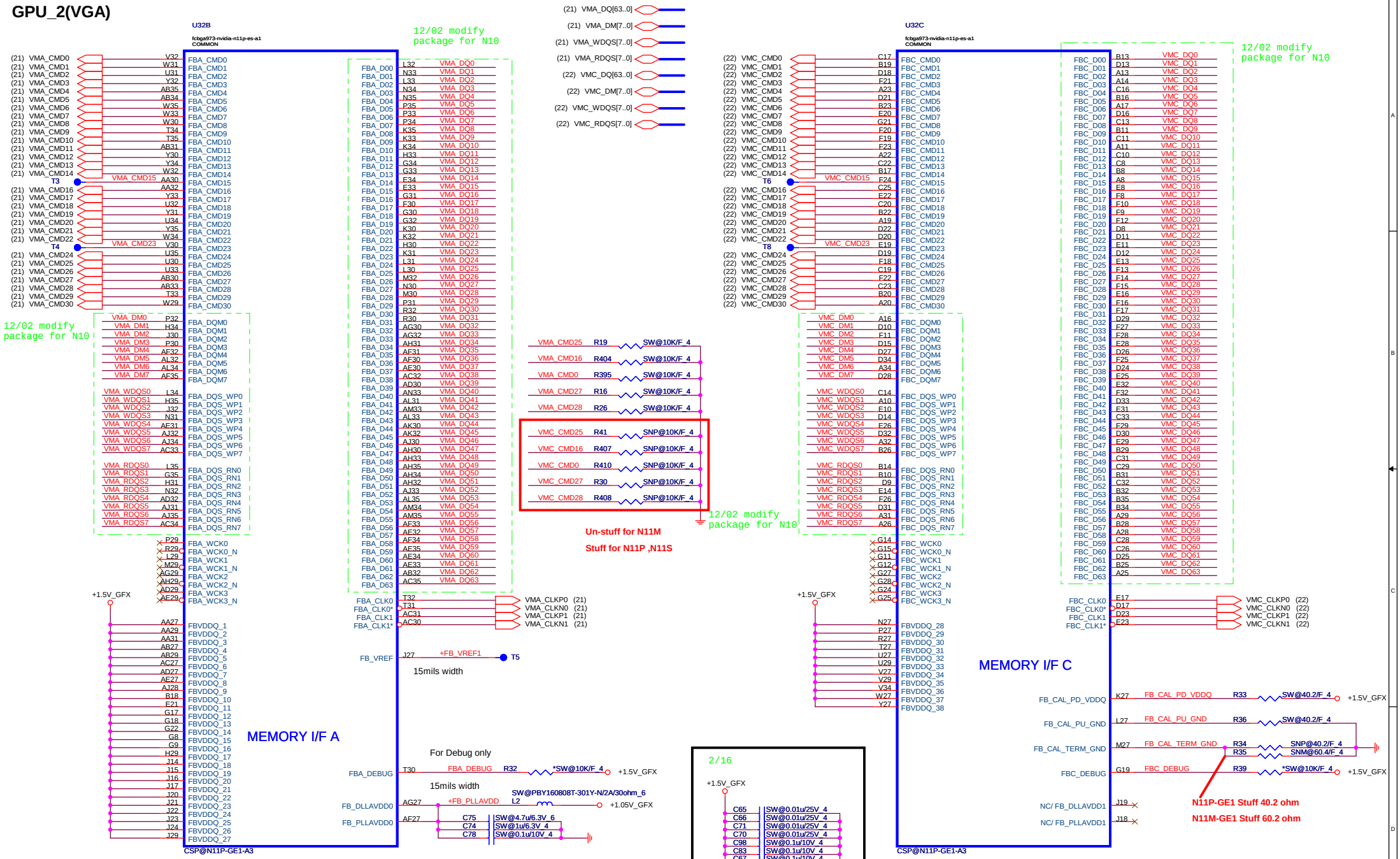
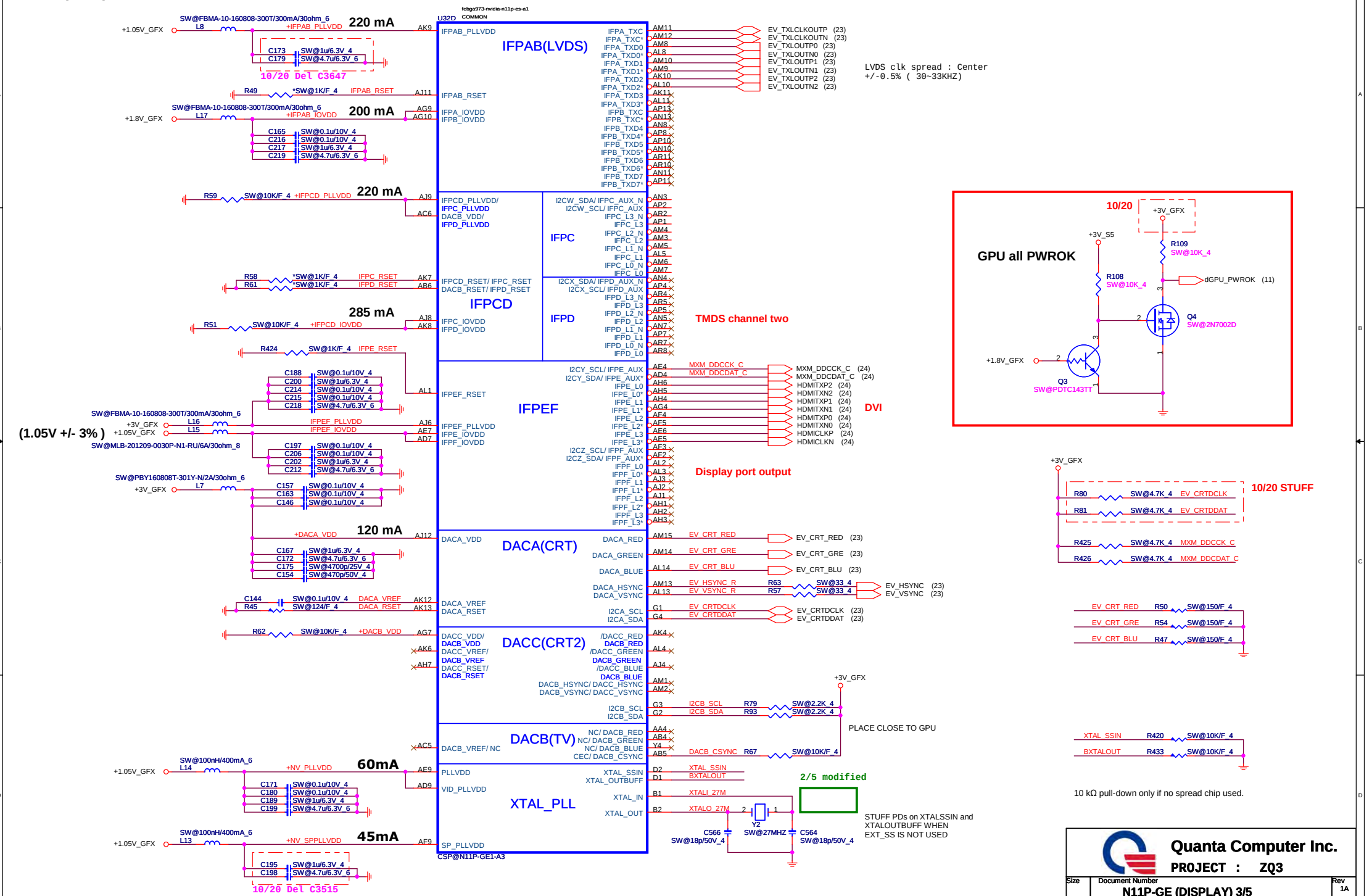
# GPU_2(VGA)


U32B
fcbga973-nvidia-n11p-es-a1
COMMON
12/02 modify package for N10
(21) VMA_DQ[63..0]
(21) VMA_DM[7..0]
(21) VMA_WDQS[7..0]
(21) VMA_RDQS[7..0]
(22) VMC_DQ[63..0]
(22) VMC_DM[7..0]
(22) VMC_WDQS[7..0]
(22) VMC_RDQS[7..0]
U32C
fcbga973-nvidia-n11p-es-a1
COMMON
12/02 modify package for N10
12/02 modify package for N10
12/02 modify package for N10
Un-stuff for N11M
Stuff for N11P ,N11S
+1.5V_GFX
FB_VREF
+FB_VREF1
T5
15mils width
For Debug only
FBA_DEBUG
R32
*SW@10K/F_4
+1.5V_GFX
15mils width
SW@PBY160808T-301Y-N/2A/30ohm_6
L2
+1.05V_GFX
FB_DLLAVDD0
FB_PLLAVDD0
+FB_PLLAVDD
C75 SW@4.7u/6.3V_6
C74 SW@1u/6.3V_4
C78 SW@0.1u/10V_4
MEMORY I/F A
CSP@N11P-GE1-A3
MEMORY I/F C
CSP@N11P-GE1-A3
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
FBC_DEBUG
NC/ FB_DLLAVDD1
NC/ FB_PLLAVDD1
R33 SW@40.2/F_4
R36 SW@40.2/F_4
R34 SNP@40.2/F_4
R35 SNM@60.4/F_4
R39 *SW@10K/F_4
N11P-GE1 Stuff 40.2 ohm
N11M-GE1 Stuff 60.2 ohm
2/16
+1.5V_GFX
C65 SW@0.01u/25V_4
C66 SW@0.01u/25V_4
C71 SW@0.01u/25V_4
C70 SW@0.01u/25V_4
C98 SW@0.1u/10V_4
C83 SW@0.1u/10V_4
C67 SW@0.1u/10V_4
C62 SW@0.047u/10V_4
C61 SW@0.047u/10V_4
C72 SW@0.047u/10V_4
C121 SW@4.7u/6.3V_6
C49 SW@4.7u/6.3V_6
All need stuff for N10P
Quanta Computer Inc.
PROJECT : ZQ3
Size
Document Number
N11P-GE (MEMORY I/F) 2/5
Rev 1A
Date: Monday, March 29, 2010
Sheet 17 of 47

# GPU_3(VGA)

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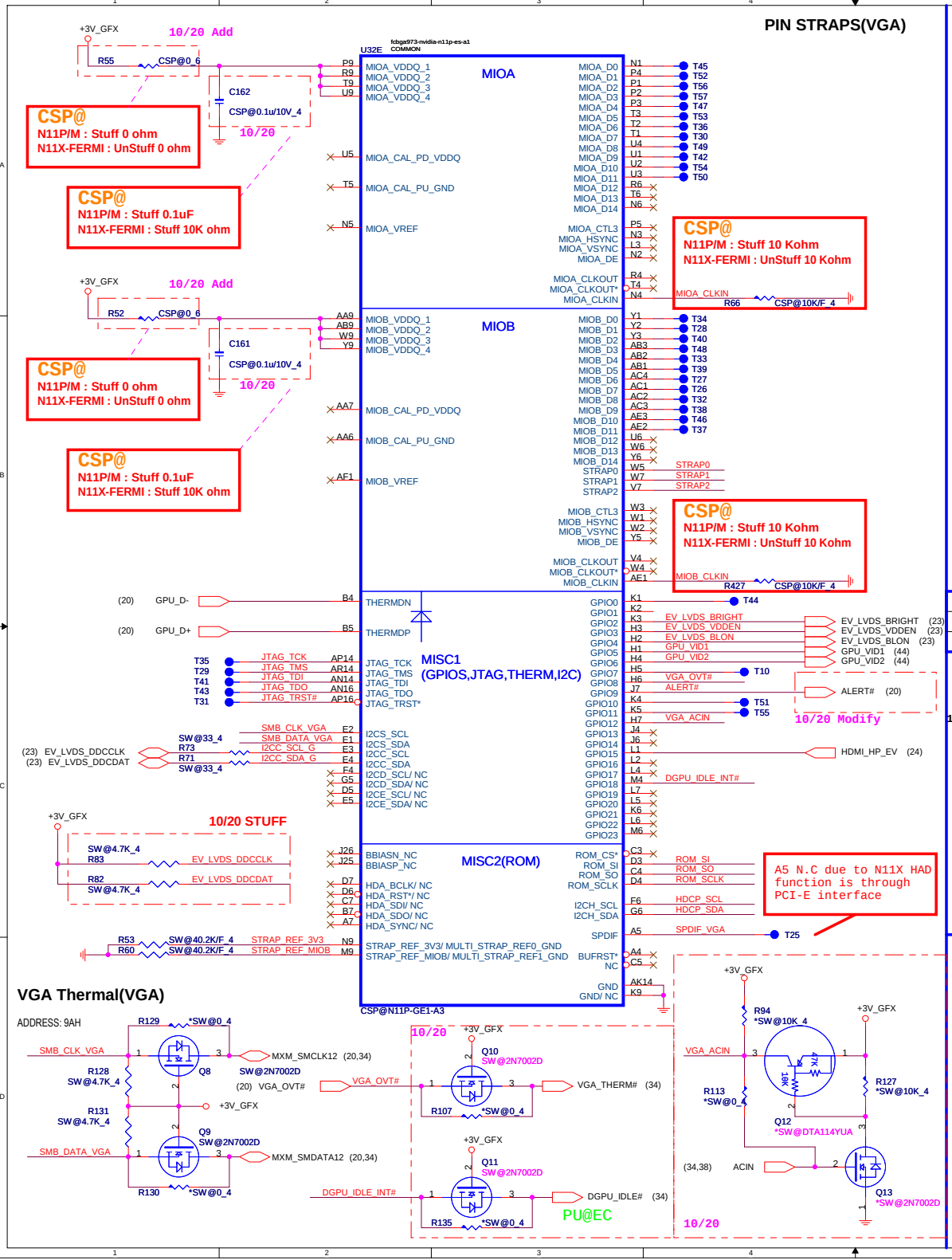
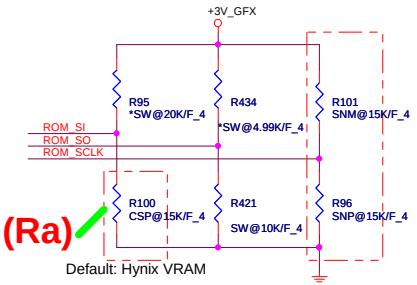
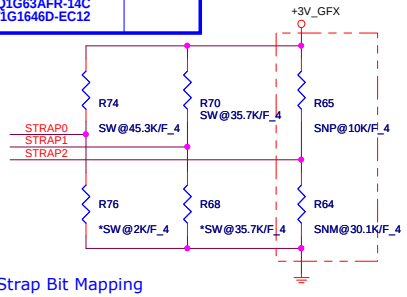



| | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 | |
|---|---|---|---|---|---|
| ROM_SO NB10X | XCLK_417 | FB_0_BAR_SIZE | SMB_ALT_ADDR | VGA_DEVICE | 0001 |
| ROM_SCLK | PCI_DEVIDE[4] | SUB_VENDOR | SLOT_CLK_CFG | PEX_PLL_EN_TERM | 0010 |
| ROM_SI | RAMCFG[3] | RAMCFG[2] | RAMCFG[1] | RAMCFG[0] | XXXX |
| STRAP2 | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0] | 1000 |
| STRAP1 | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] | 3GIO_PADCFG[0] | 0001 |
| STRAP0 | USER[3] | USER[2] | USER[1] | USER[0] | 1111 |

VRAM Configuration Table

| RAMCFG [3:0] | DESCRIPTION | Vendor | Vendor P/N | ROM_SI | (Ra) |
|---|---|---|---|---|---|
| 0000 | | Reserved | | PD 10K | AKD58GGT^01 |
| 0001 | DDR3 64Mx16x8, 128bit, 1GB,800MHz | Qimonda | IDGH1G-04A1F1C-16X | PD 15K | AKD5LZGTW00 |
| 0010 | DDR3 64Mx16x8, 128bit, 1GB,800MHz | Hynix | H5TQ1G63BFR-12C | PD 20K | AKD5LGGT502 |
| 0011 | DDR3 64Mx16x8, 128bit, 1GB,800MHz | Samsung | K4W1G1646E-HC12 | | |
| 0101 | | Reserved | | | |
| 0110 | | | | | |
| XXXX | DDR3 64Mx16x8, 128bit, 1GB,667MHz | Hynix | H5TQ1G63AFR-14C | | |
| XXXX | DDR3 64Mx16x8, 128bit, 1GB,667MHz | Samsung | K4W1G1646D-EC12 | | |

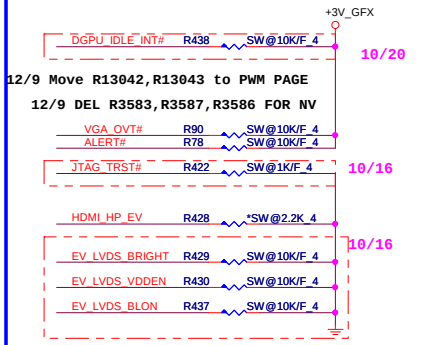



Logical Strap Bit Mapping

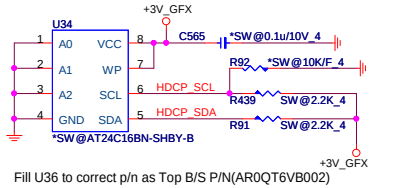
| | PU | PD |
|---|---|---|
| 5K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 25K | 1100 | 0100 |
| 30K | 1101 | 0101 |
| 35K | 1110 | 0110 |
| 45K | 1111 | 0111 |

| CHIP | ROM_SCLK | STRAP2 | PCI_DEVID |
|---|---|---|---|
| N11M-GE1 | PU 15K | PD 30K | 0x0A75 |
| N11P-GE1 | PD 15K | PU 10K | 0x0A29 |




4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

## HDCP ROM (VGA)




Fill U36 to correct p/n as Top B/S P/N(AR0QT6VB002)

| DHCP ROM | |
|---|---|
| HDCP_SCL | Low: Crypto ROM<br>Hi: I2C ROM |

HDCP ROM reserve , Due to N11x had support internal HDCP function.

## GPIO ASSIGNMENTS

| GPIO | I/O | ACTIVE | USAGE |
|---|---|---|---|
| 0 | N/A | N/A | |
| 1 | IN | N/A | Hot plug detect for IFP link C |
| 2 | OUT | HIGH | PANEL BACKLIGHT PWM |
| 3 | OUT | HIGH | PANEL POWER ENABLE |
| 4 | OUT | HIGH | PANEL BACKLIGHT ENABLE |
| 5 | OUT | N/A | NVVDD VID0 |
| 6 | OUT | N/A | NVVDD VID1 |
| 7 | OUT | N/A | NVVDD VID2 11/13 |
| 8 | I/O | LOW | OVERT |
| 9 | I/O | LOW | ALERT |
| 10 | OUT | N/A | FBVREF SELECT |
| 11 | OUT | N/A | SLI SYNC0 |
| 12 | IN | N/A | PWR_LEVEL 11/13 |
| 13 | OUT | N/A | MEM_VID or power supply control |
| 14 | OUT | N/A | PS CONTROL |

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PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | N11P-GE (GPIO&STRAPS) 4/5 | 1A |

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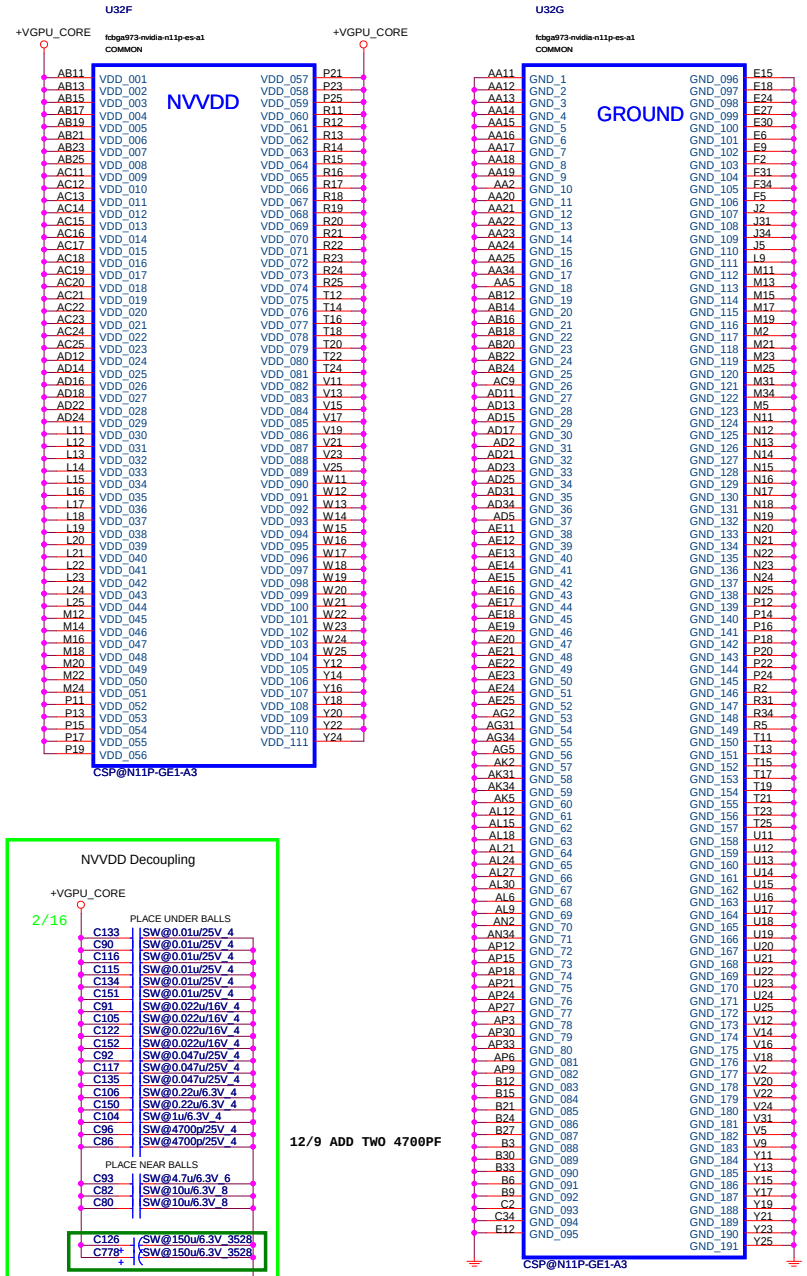
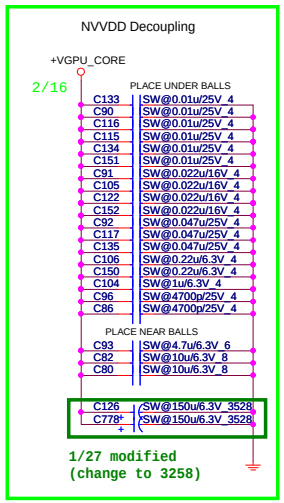
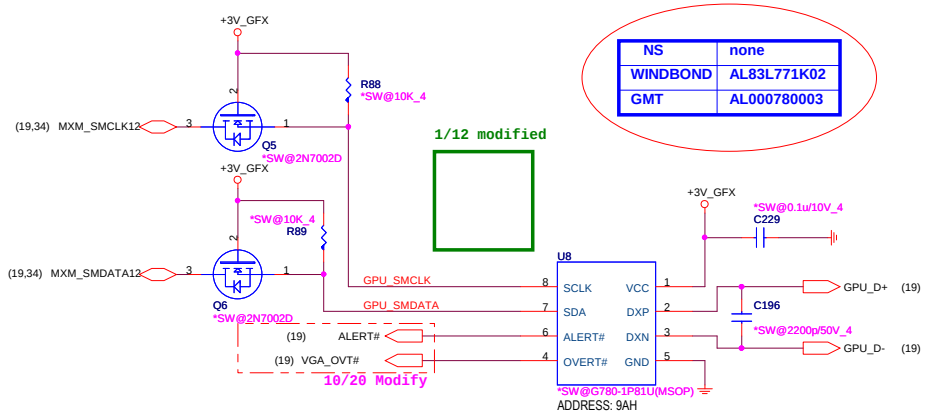
# GPU_4(VGA)



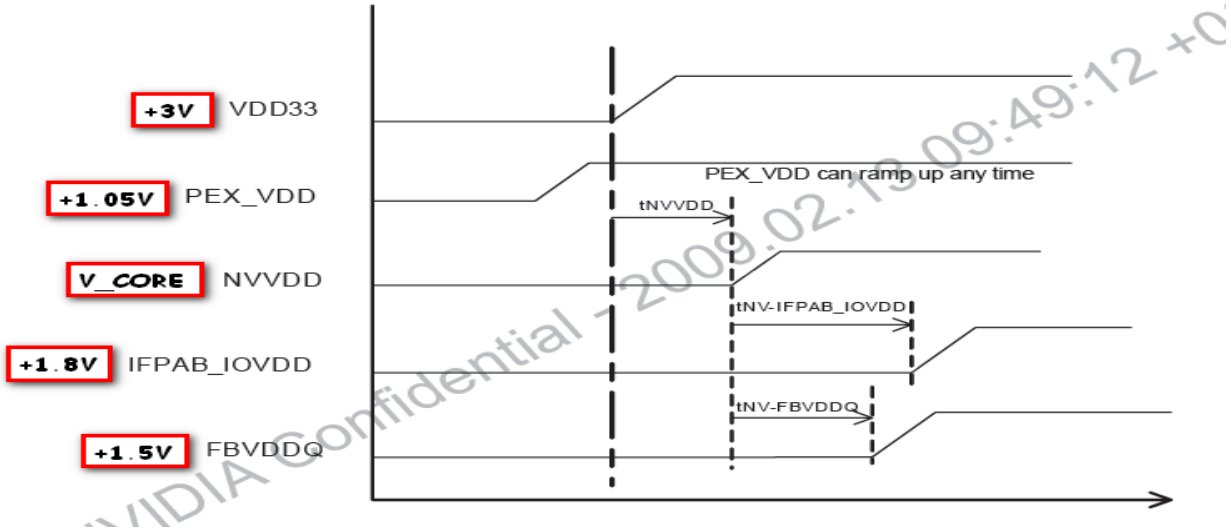




12/9 ADD TWO 4700PF

## Thermal Sensor(VGA)




| NS | none |
|---|---|
| WINDBOND | AL83L771K02 |
| GMT | AL000780003 |




NVIDIA Confidential - 2009.02.19 09:49:12 +0

Quanta Computer Inc.

PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | N11P-GE (POWER & GND&THM) 5/5 | 1A |

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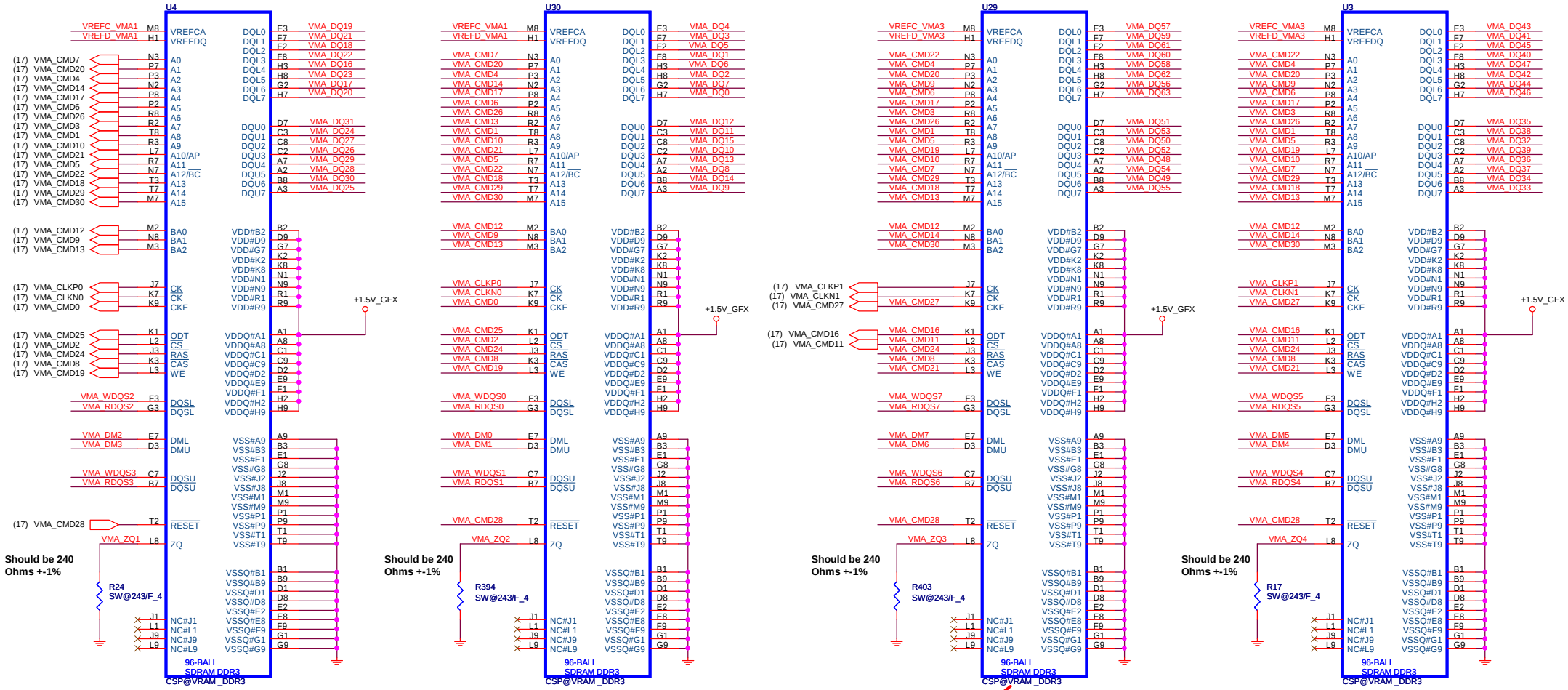
# VRAM_A(VGA)

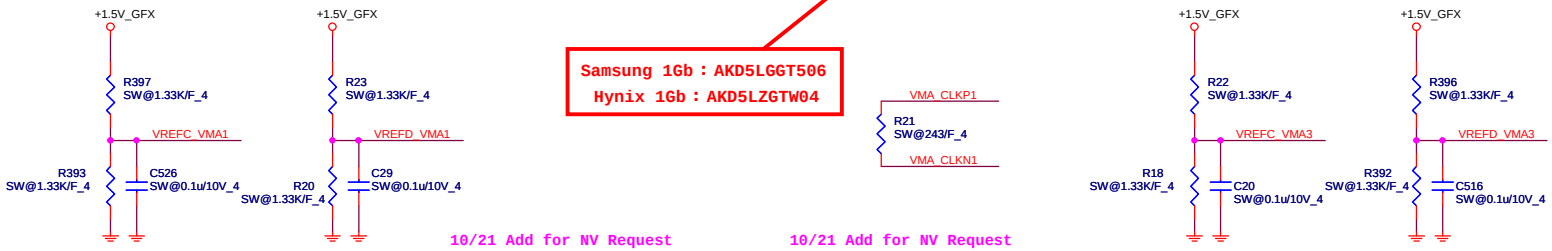
(17) VMA_DQ[63..0]
(17) VMA_DM[7..0]
(17) VMA_WDQS[7..0]
(17) VMA_RDQS[7..0]

# CHANNEL A: 256MB/512MB DDR3

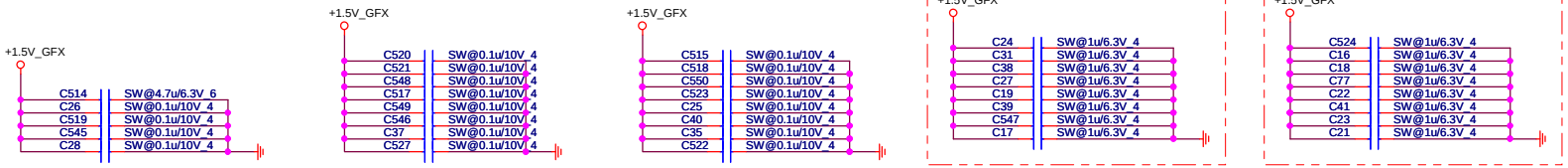
(17,22,46) +1.5V_GFX




Samsung 1Gb : AKD5LGGT506
Hynix 1Gb : AKD5LZGTW04




12/9 NV recommend 0.1uf x 5, 1uf x 4 per DDR3
DEL C3627,C3684,C3681,C3662 ,C3678,C3692
C3690,C3695,C3685 FOR NV suggestion




**Quanta Computer Inc.**

PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | N11P-GE VRAM-1(DDR3 BGA96) | 1A |

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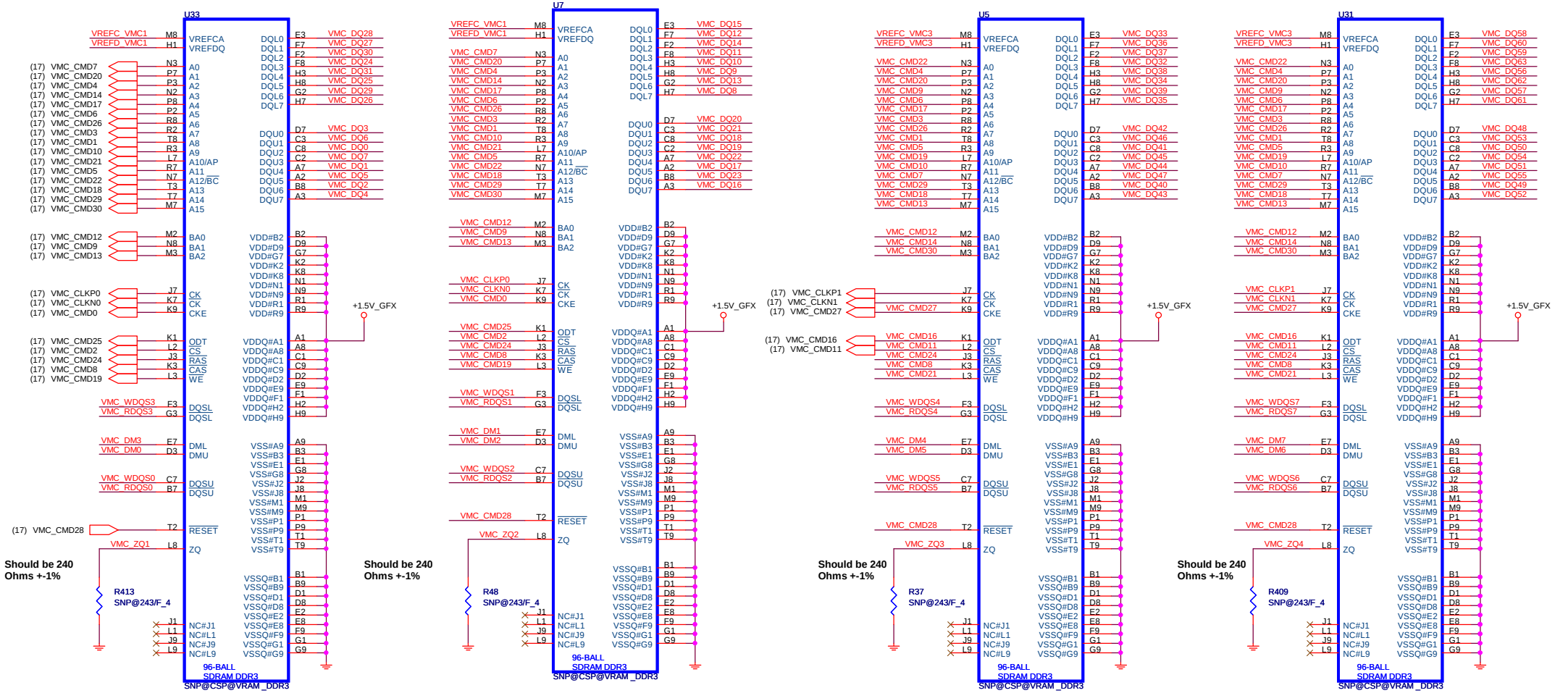
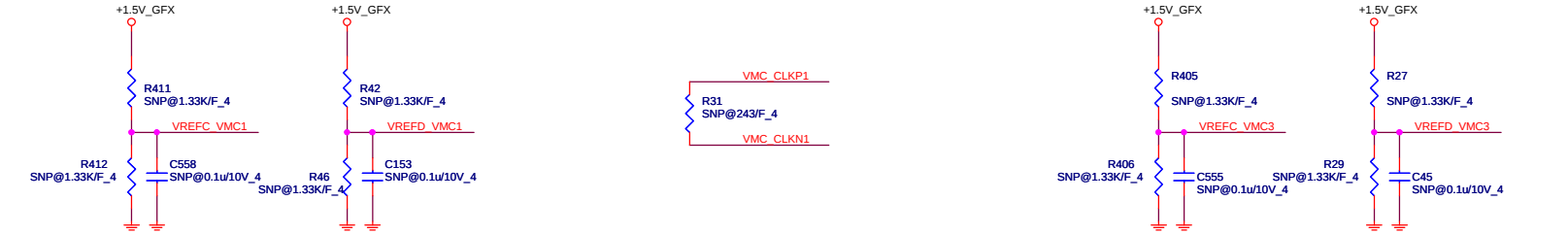
VRAM_C(VGA)

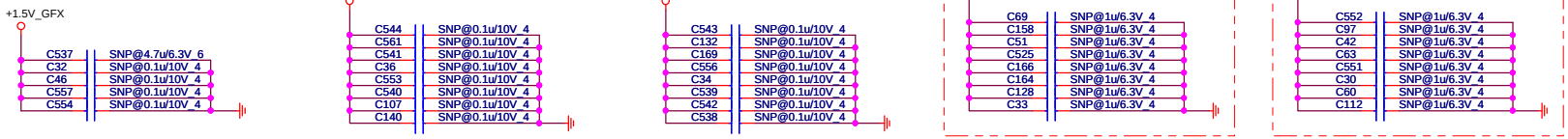
# CHANNEL B: 256MB/512MB DDR3




12/9 NV recommend 0.1uf x 5, 1uf x 4 per DDR3

DEL C3585,C3637,C3653,C3655,C3665 FOR NV recommend




Quanta Computer Inc.

PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | N11P-GE VRAM-2(DDR3 BGA96) | 1A |

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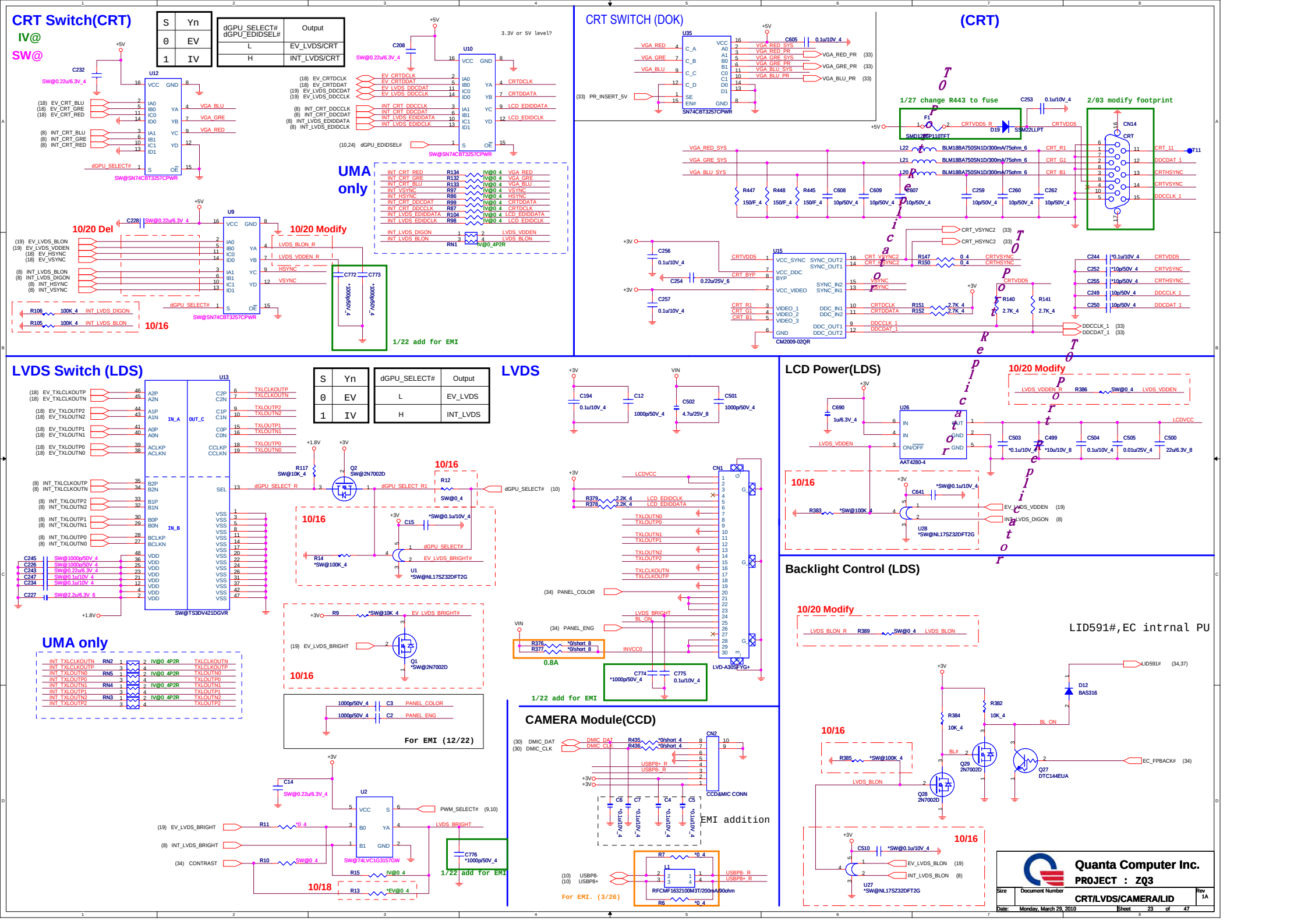
CRT Switch(CRT)
IV@
SW@
S Yn
0 EV
1 IV
dGPU_SELECT# dGPU_EDIDSEL# Output
L EV_LVDS/CRT
H INT_LVDS/CRT
3.3V or 5V level?
U12
U10
U9
SW@SN74CBT3257CPWR
10/20 Del
10/20 Modify
UMA only
10/16
1/22 add for EMI
CRT SWITCH (DOK)
U35
SN74CBT3257CPWR
(CRT)
1/27 change R443 to fuse
2/03 modify footprint
CN14
CRT
U15
CM2009-02QR
LVDS Switch (LDS)
U13
SW@TS3DV421DGVR
S Yn
0 EV
1 IV
dGPU_SELECT# Output
L EV_LVDS
H INT_LVDS
LVDS
LCD Power(LDS)
10/20 Modify
U26
AAT4280-4
U28
*SW@NL17SZ32DFT2G
Backlight Control (LDS)
10/20 Modify
LID591#,EC intrnal PU
D12
BAS316
Q29
2N7002D
Q28
2N7002D
Q27
DTC144EUA
U27
*SW@NL17SZ32DFT2G
UMA only
For EMI (12/22)
U2
SW@74LVC1G3157GW
10/18
1/22 add for EMI
CAMERA Module(CCD)
CN2
CCD&MIC CONN
EMI addition
For EMI. (3/26)
Quanta Computer Inc.
PROJECT : ZQ3
Size
Document Number
CRT/LVDS/CAMERA/LID
Rev 1A
Date: Monday, March 29, 2010
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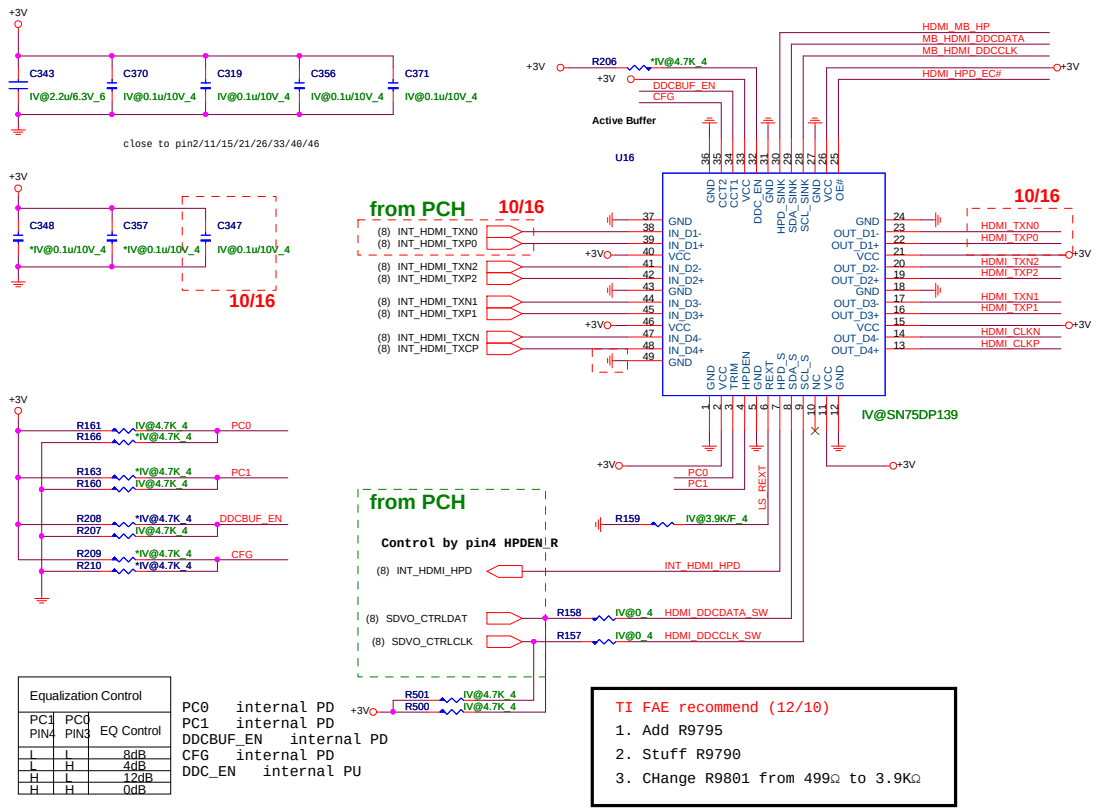
# I@ HDMI LEVEL SHIFTER(DOK)

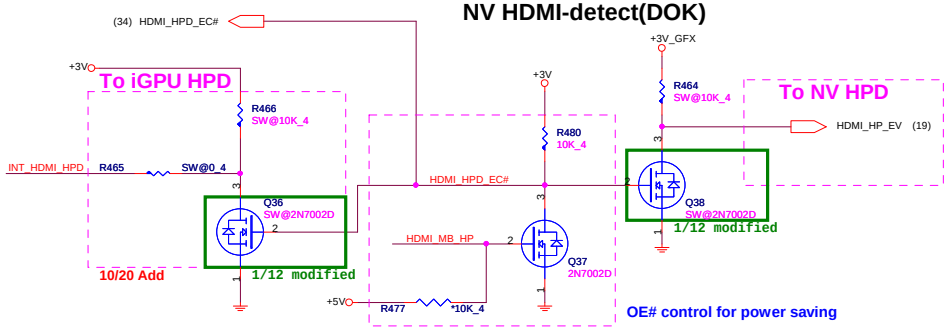



| Equalization Control | | |
|---|---|---|
| PC1 PIN4 | PC0 PIN3 | EQ Control |
| L | L | 8dB |
| L | H | 4dB |
| H | L | 12dB |
| H | H | 0dB |

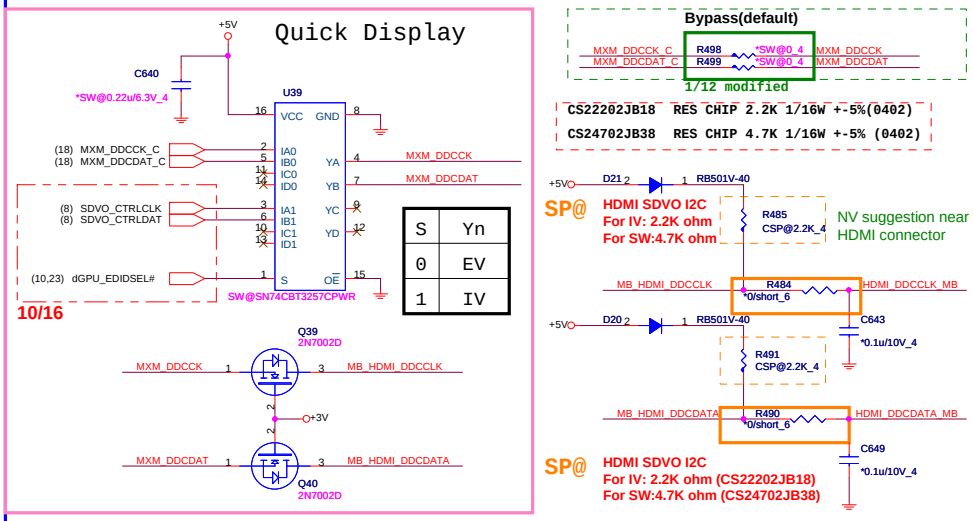
PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

TI FAE recommend (12/10)
1. Add R9795
2. Stuff R9790
3. CHange R9801 from 499Ω to 3.9KΩ

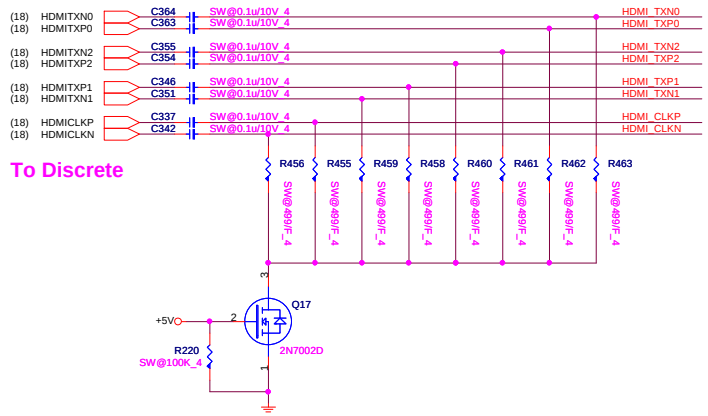
# NV HDMI-detect(DOK)



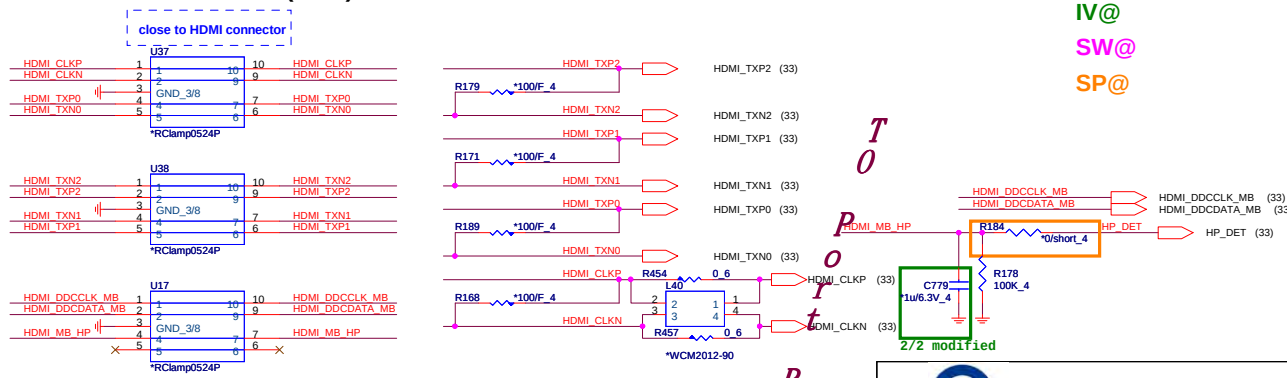

# SDVO I2C Control(DOK)




# Switchable Graphic HDMI source(DOK)




# ESD Protect(DOK)




Quanta Computer Inc.
PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | DVI (PS8101) | 1A |

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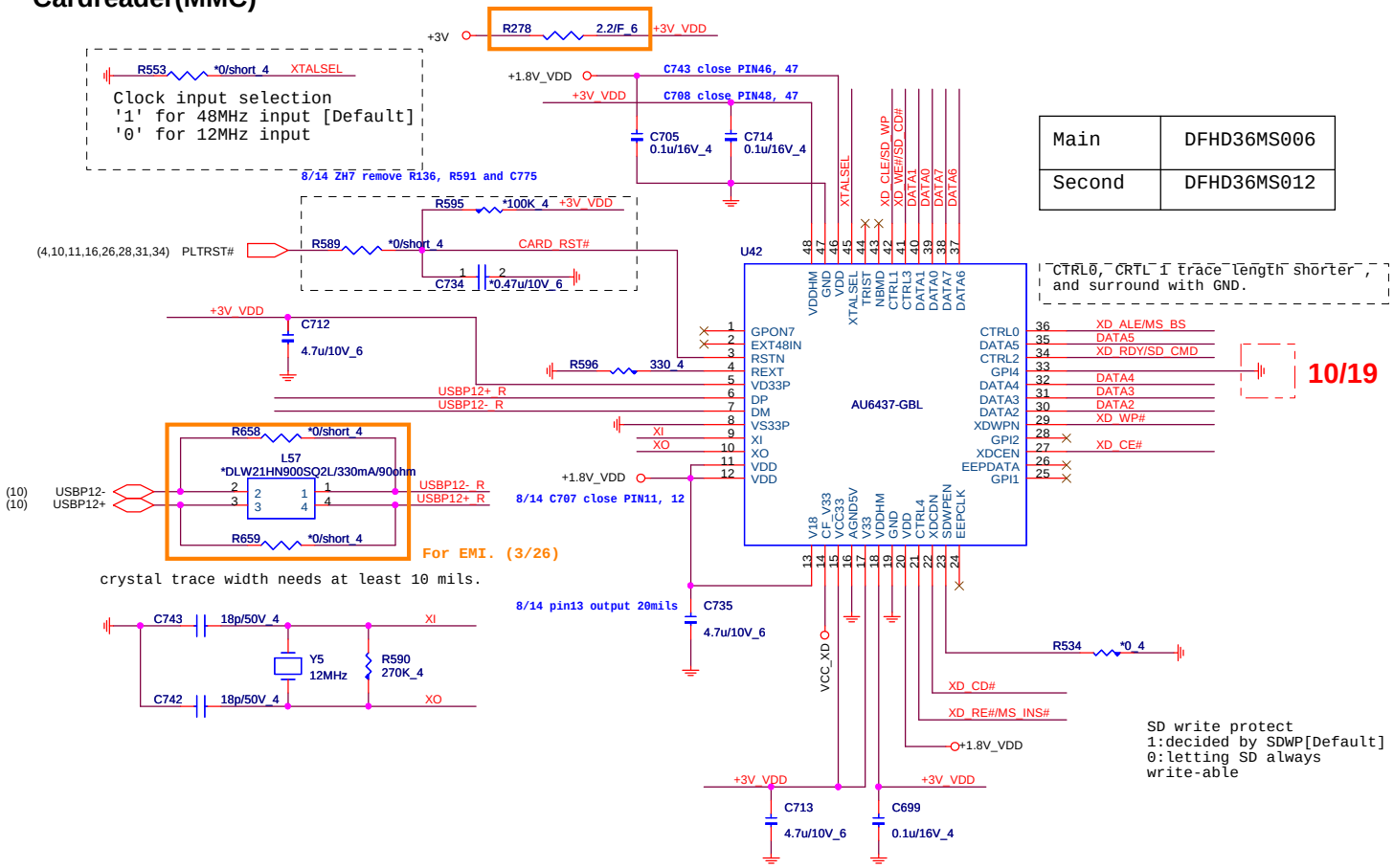
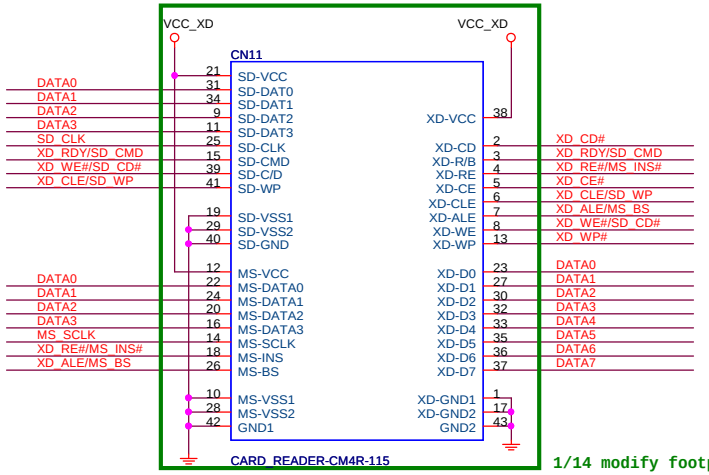
# Cardreader(MMC)

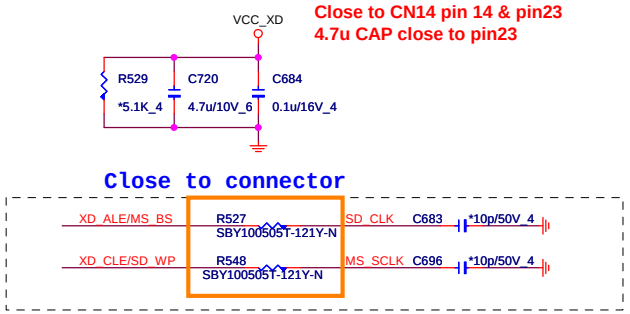



| | |
|---|---|
| Main | DFHD36MS006 |
| Second | DFHD36MS012 |

# 4 IN 1 CARD READER (MMC)

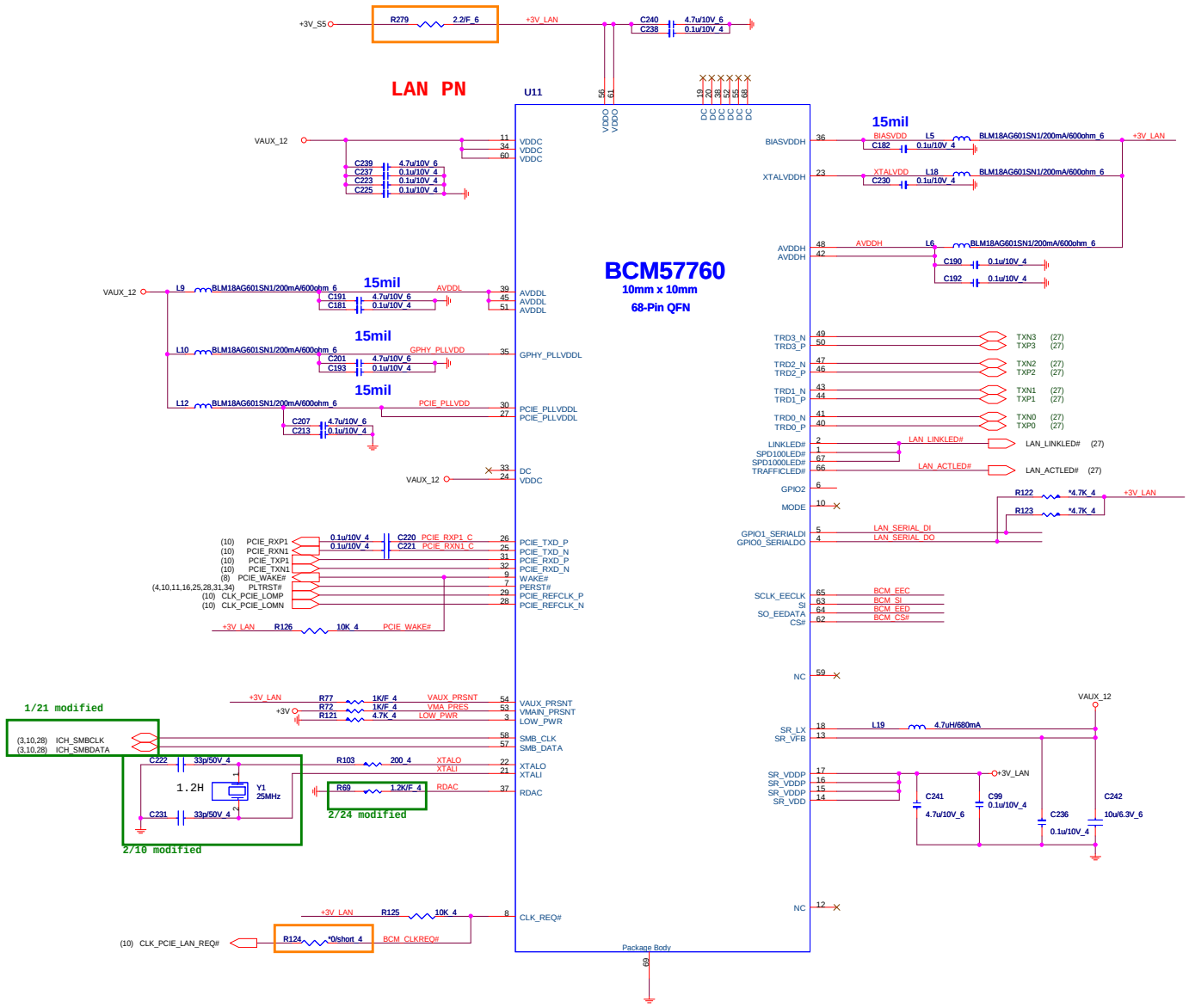



1/14 modify footprint.

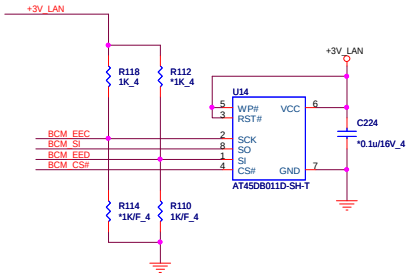



| | | | |
|---|---|---|---|
| Quanta Computer Inc. | | | |
| PROJECT : ZQ3 | | | |
| Size | Document Number | AU6437 CardReader | Rev 1A |
| Date: Monday, March 29, 2010 | Sheet 25 of 47 | | |

# Giga-LAN BCM57760(LAN)




## Flash (1M) for ASF2.0

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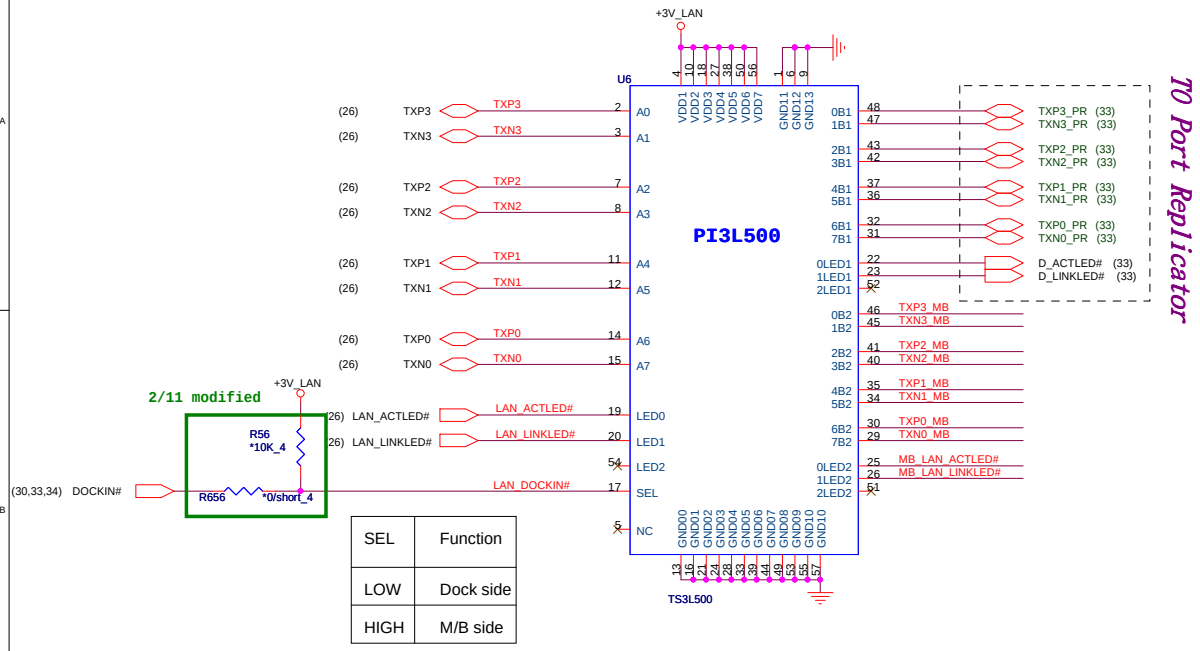
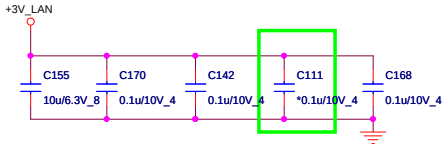
| | | | |
|---|---|---|---|
| Quanta Computer Inc. | | | |
| PROJECT : ZQ3 | | | |
| Size | Document Number | LAN (AR8151) | Rev 1A |
| Date: Monday, March 29, 2010 | Sheet 26 of 47 | | |

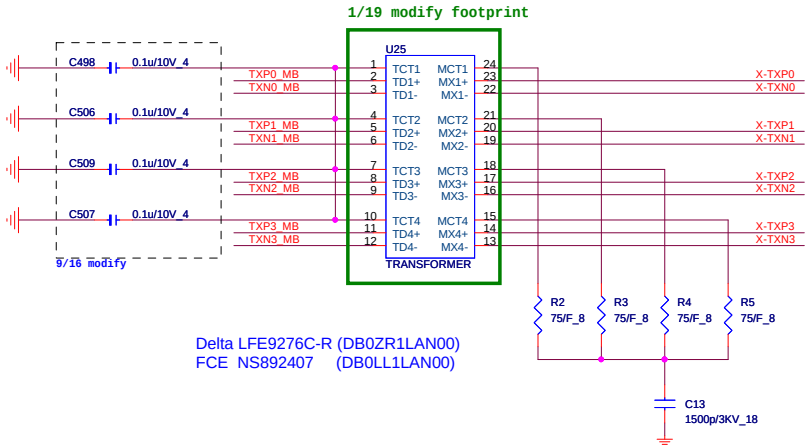
# LAN SWITCH (DOK)




| SEL | Function |
|---|---|
| LOW | Dock side |
| HIGH | M/B side |

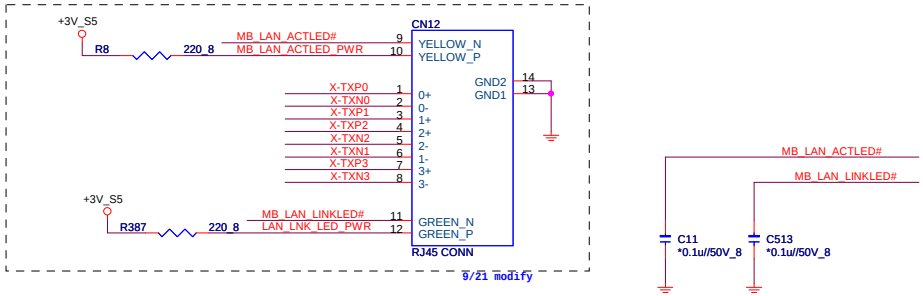



# TRANSFORMER (LAN)




Delta LFE9276C-R (DB0ZR1LAN00)
FCE NS892407 (DB0LL1LAN00)

# RJ45(LAN)




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZQ3 | | |
| Size | Document Number: LAN SWITCH/TRANSFORMER/RJ45/BT | Rev 1A |
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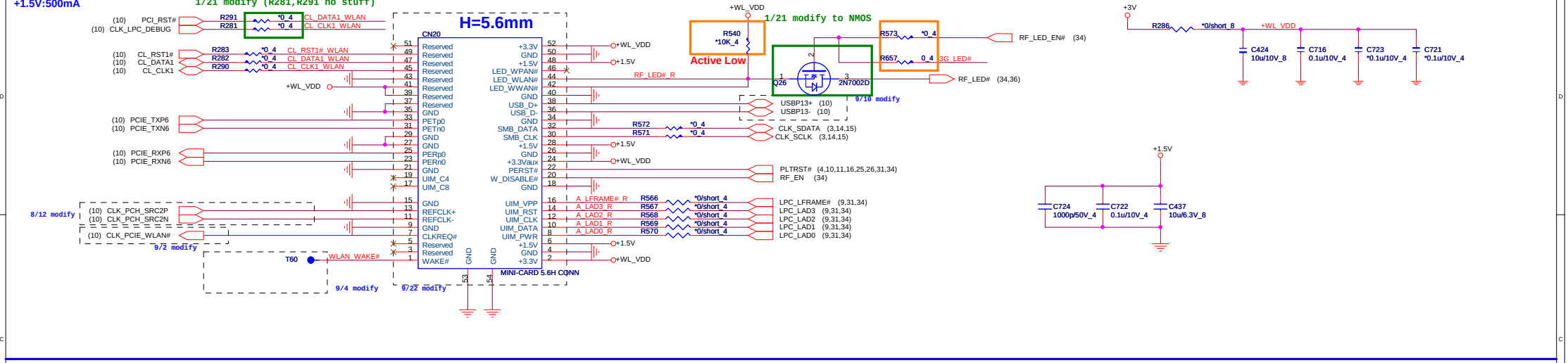
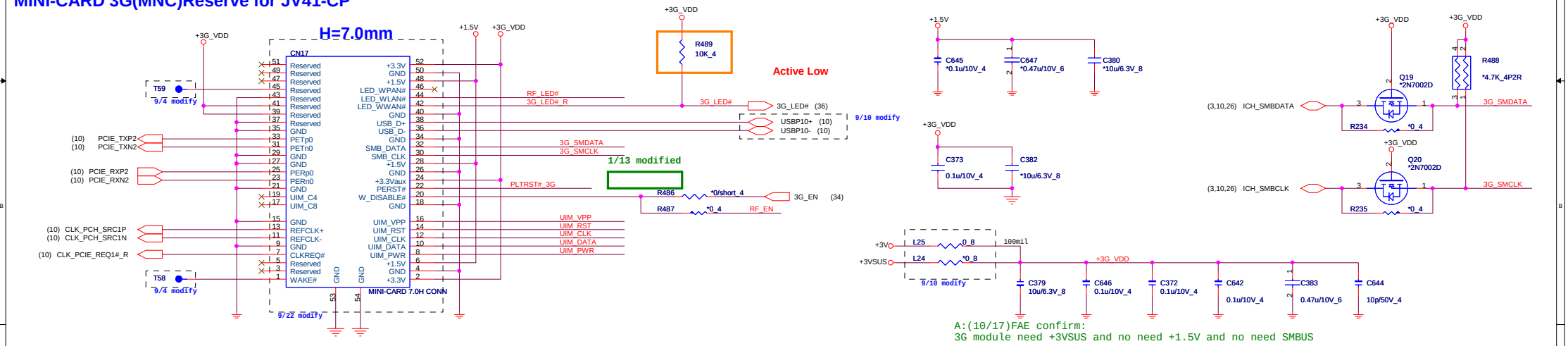
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

## MINI-CARD WLAN/WMAX(MPC)




## MINI-CARD 3G(MNC)Reserve for JV41-CP




## SIM CARD FFC connector(RFM)

Quanta Computer Inc.
PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | Mini-Card/WL/3G/SIM | 1A |

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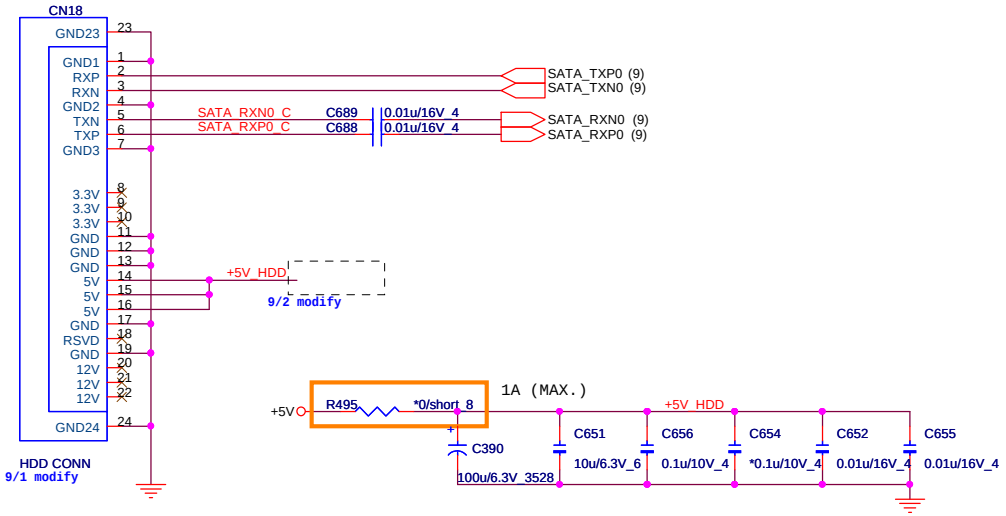
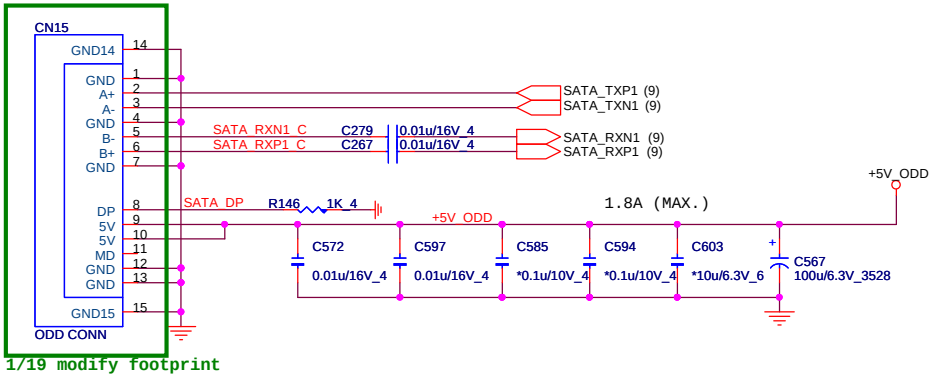
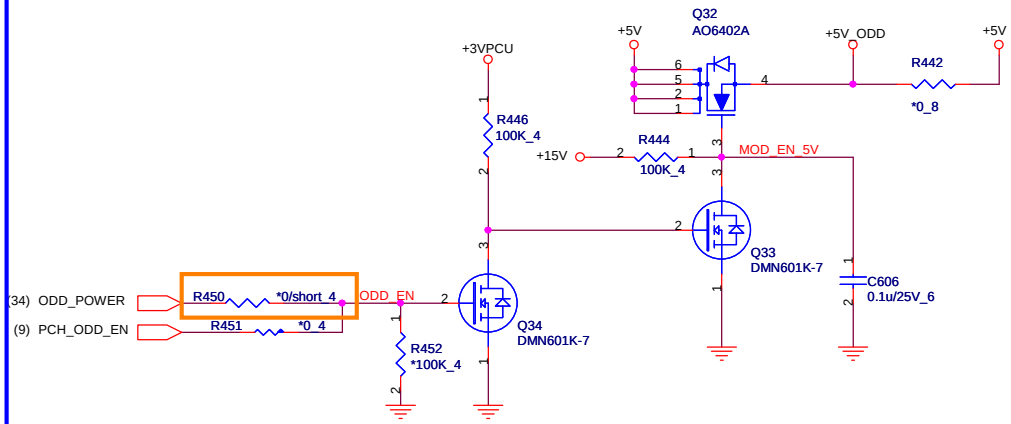
## SATA HDD(HDD)




## SATA ODD (ODD)



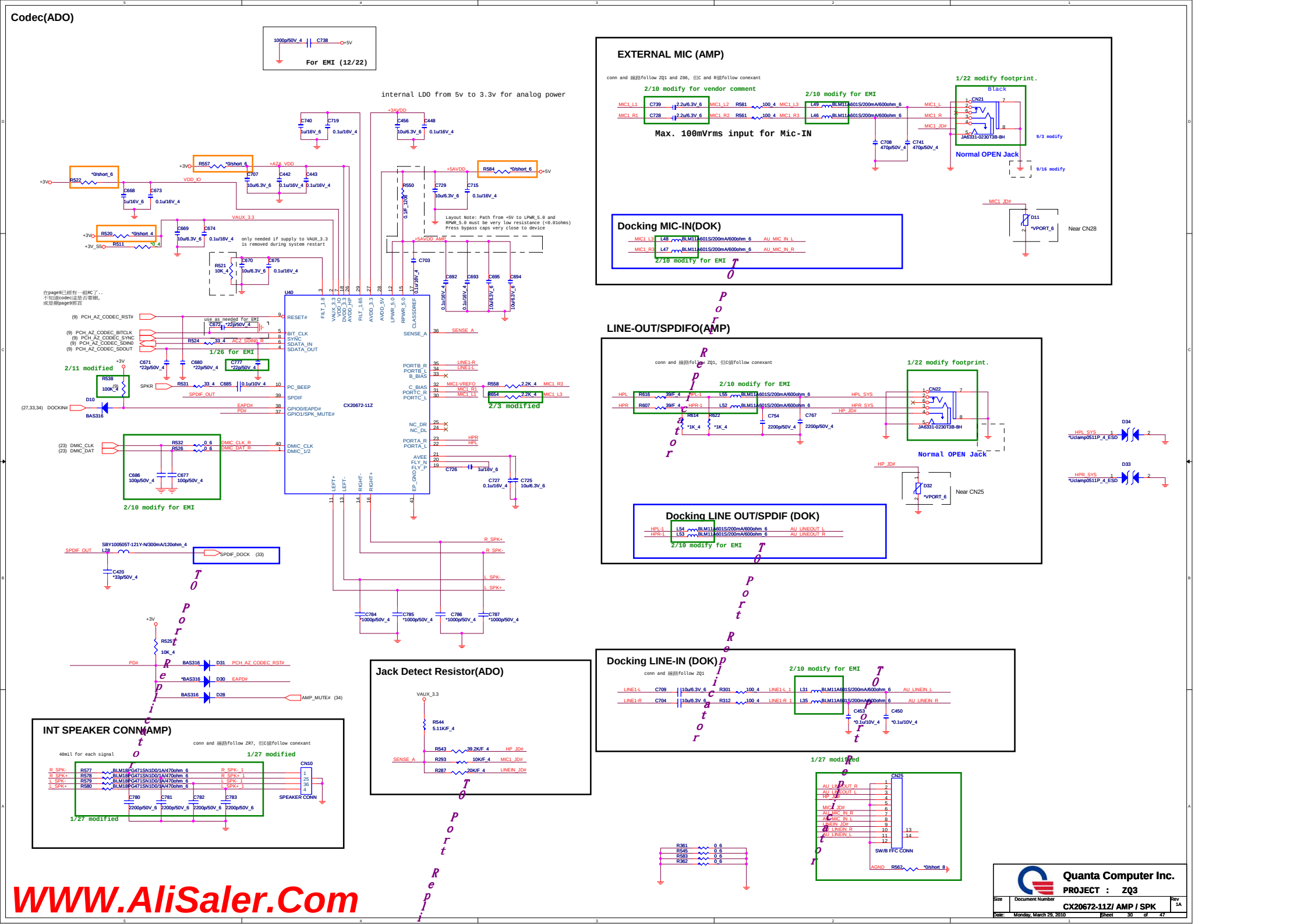

## ODD POWER(ODD)




Connect to PCH(GPIO21) pin Y9
and EC pin28(GPIO53)

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZQ3 | | |
| Size | Document Number | Rev |
| | SATA-HDD/ODD/HOLE | 1A |
| Date: Monday, March 29, 2010 | Sheet 29 of 47 | |

# Codec(ADO)

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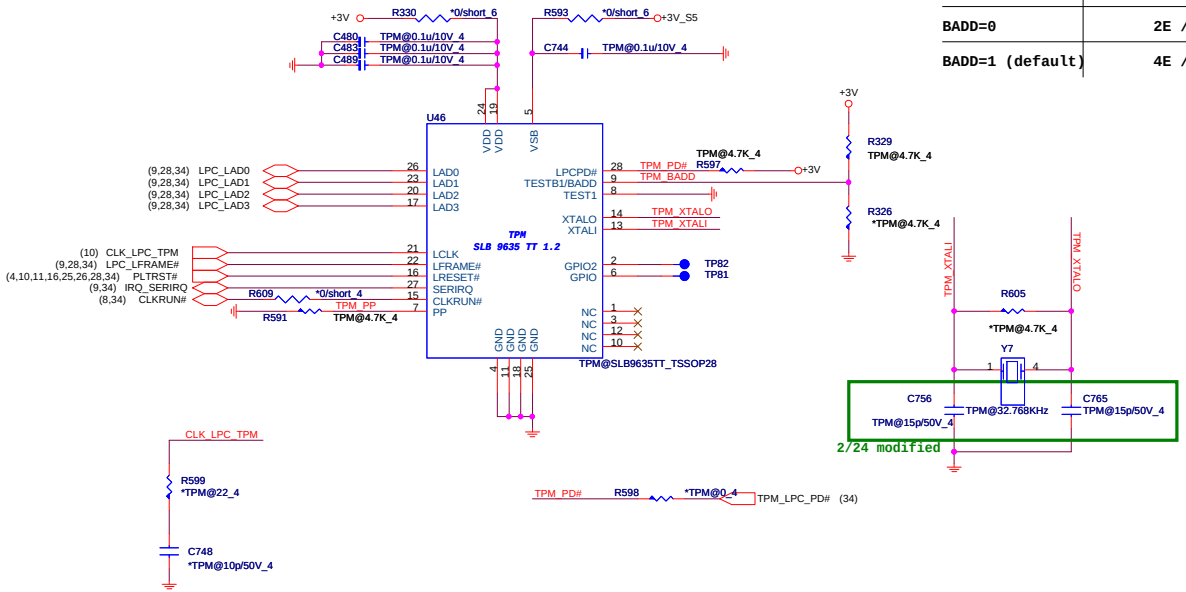
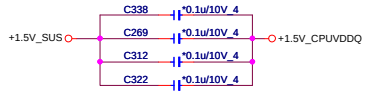
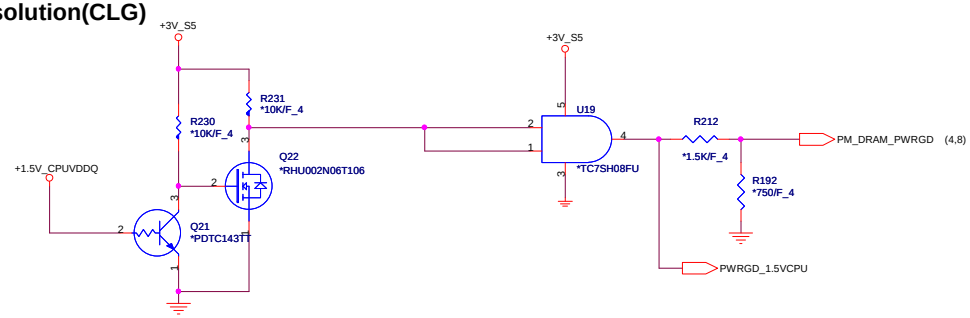
## (TPM)

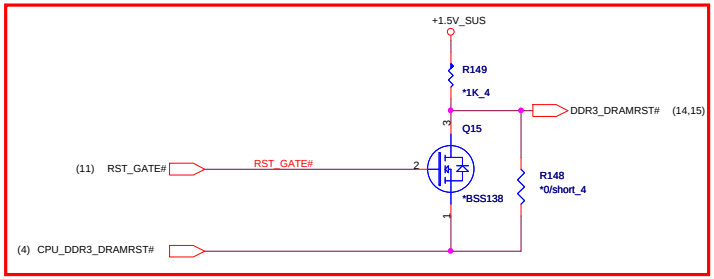
| | Resiger Base Address |
|---|---|
| BADD=0 | 2E / 2F |
| BADD=1 (default) | 4E / 4F |

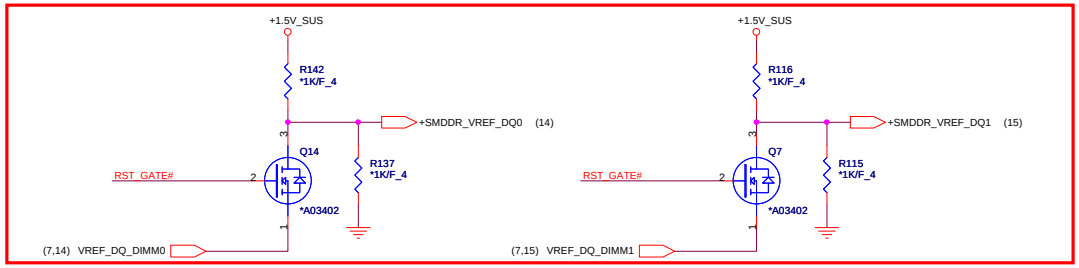



## S3 leakage solution(CLG)




Quanta Computer Inc.

PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | Mini-Card/WL/3G/SIM | 1A |

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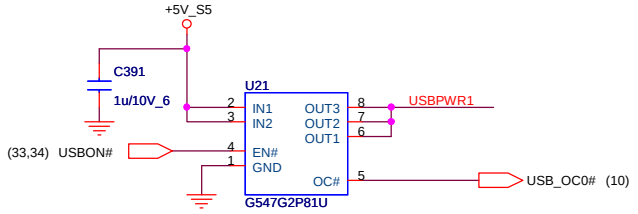
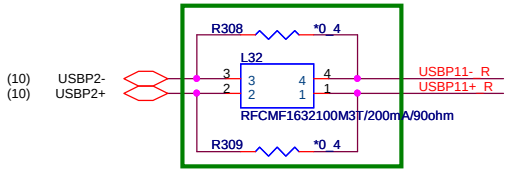
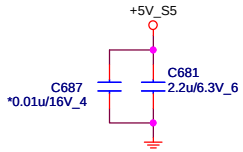
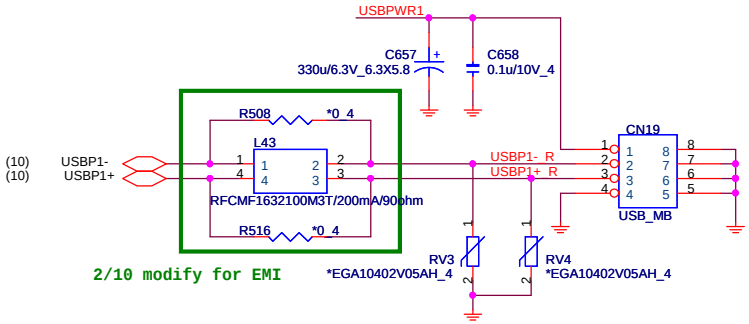


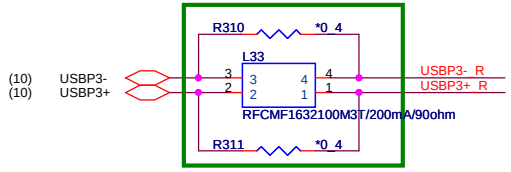




2/10 modify for EMI

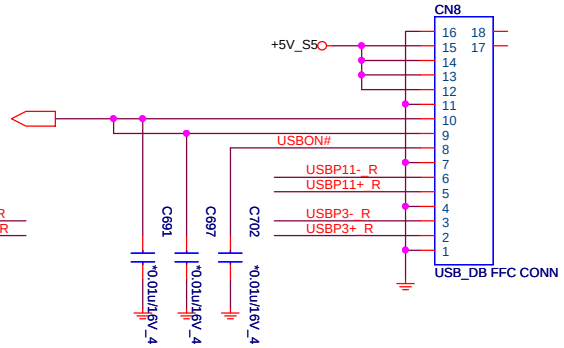


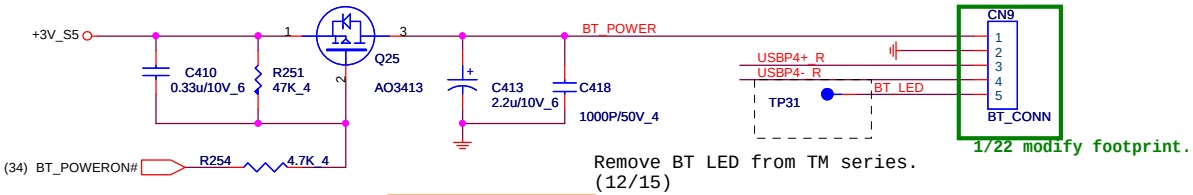




2/10 modify for EMI



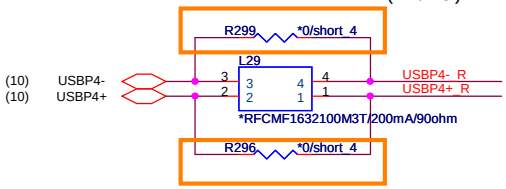

2/10 modify for EMI




Remove BT LED from TM series.
(12/15)

1/22 modify footprint.




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZQ3 | | |
| Size | Document Number | Rev |
| | eSATA/USB | 1A |
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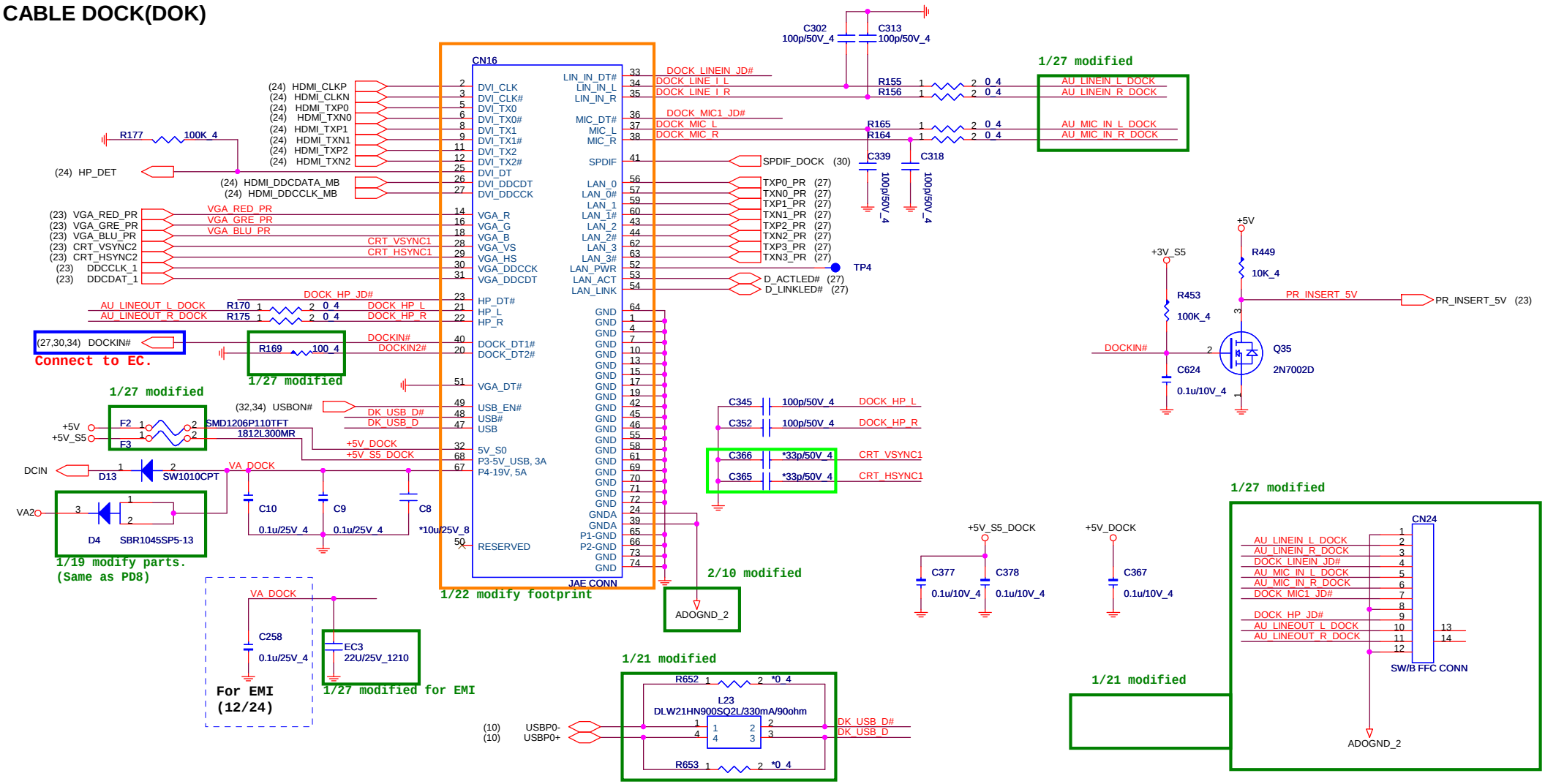
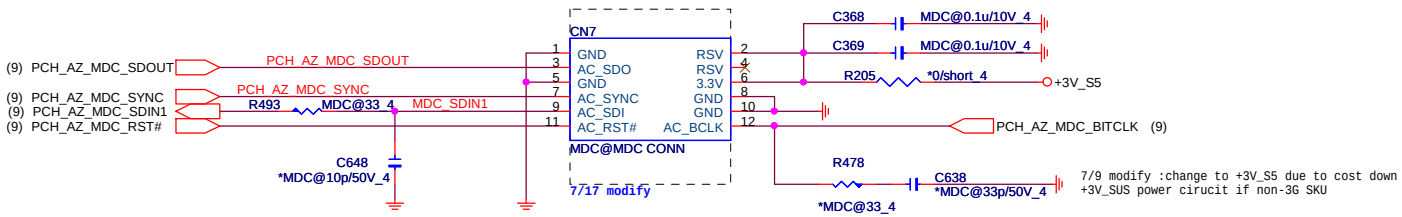
# CABLE DOCK(DOK)




# MDC(MDM)




Quanta Computer Inc.

PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | Docking | 1A |

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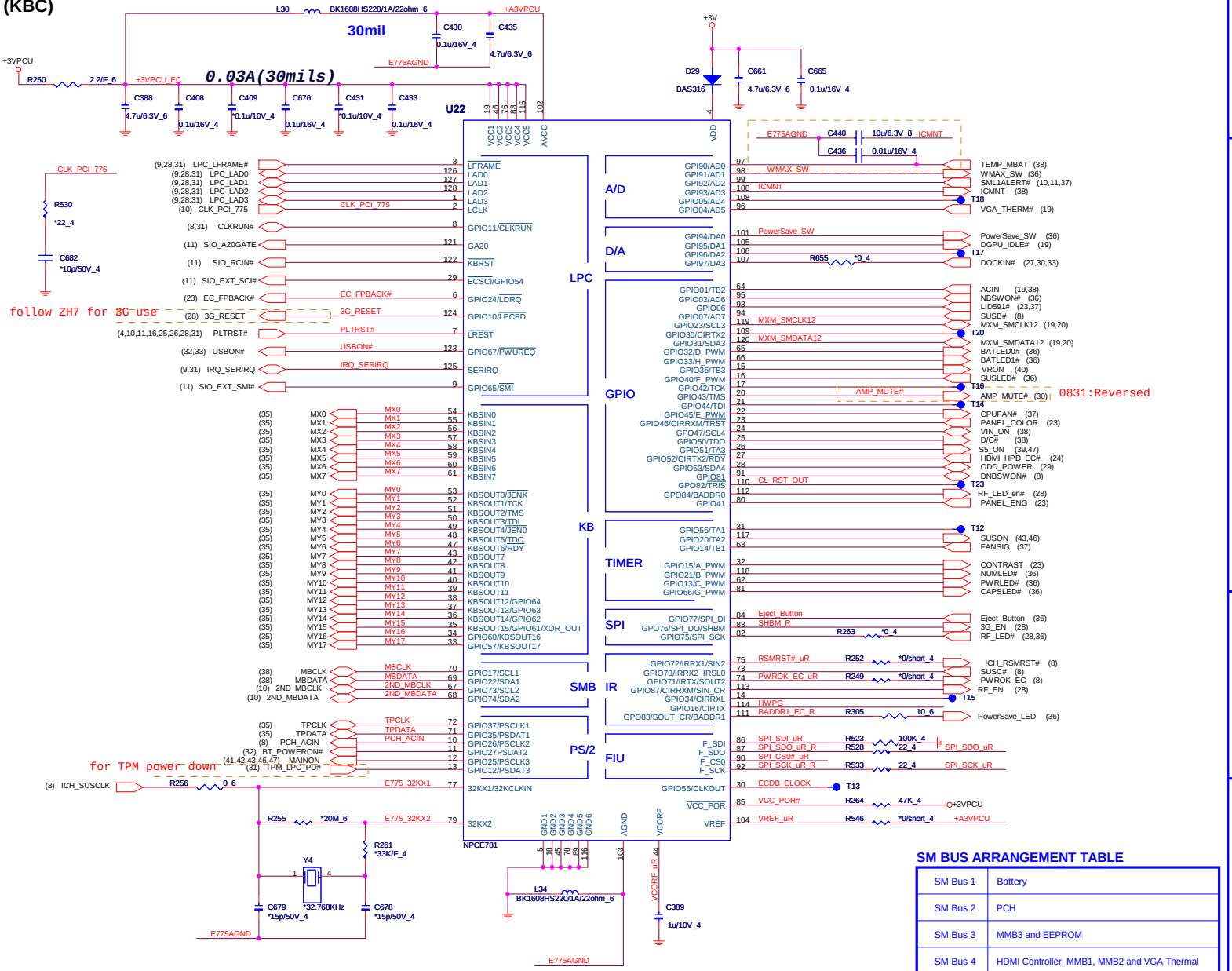
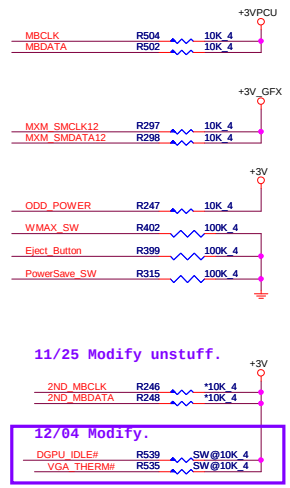
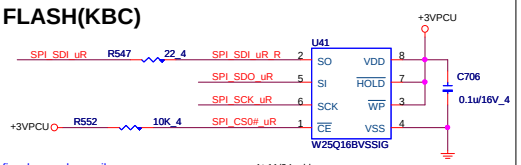
# EC (KBC)




## SM BUS PU(KBC)




## SPI FLASH(KBC)

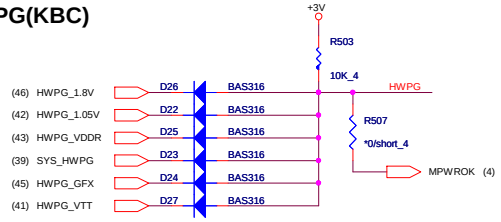


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

At 11/24 add

| | | |
|---|---|---|
| Winbond W25X16AVSSIG | | AKE382P0N01 |
| MXIC | MX25L1605AM2C-15G | AKE37FP0Z13 |
| EON | EN25F16-100HIP | AKE38ZA0Q00 |
| AMIC | A25L016 | AKE38ZN0800 |

## HWPG(KBC)



## INTERNAL KEYBOARD STRIP SET(KBC)

Quanta Computer Inc.
PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | WPCE775C_0DG & FLASH | 1A |

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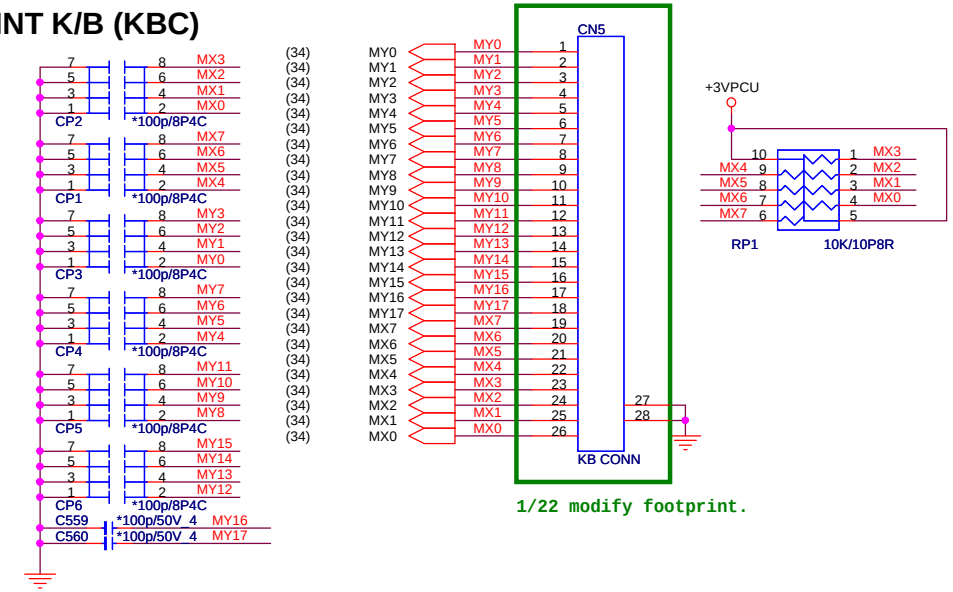
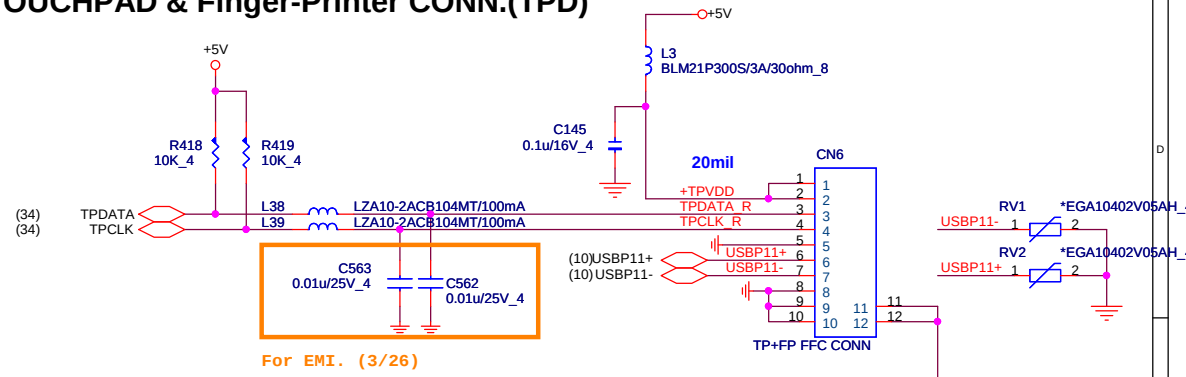
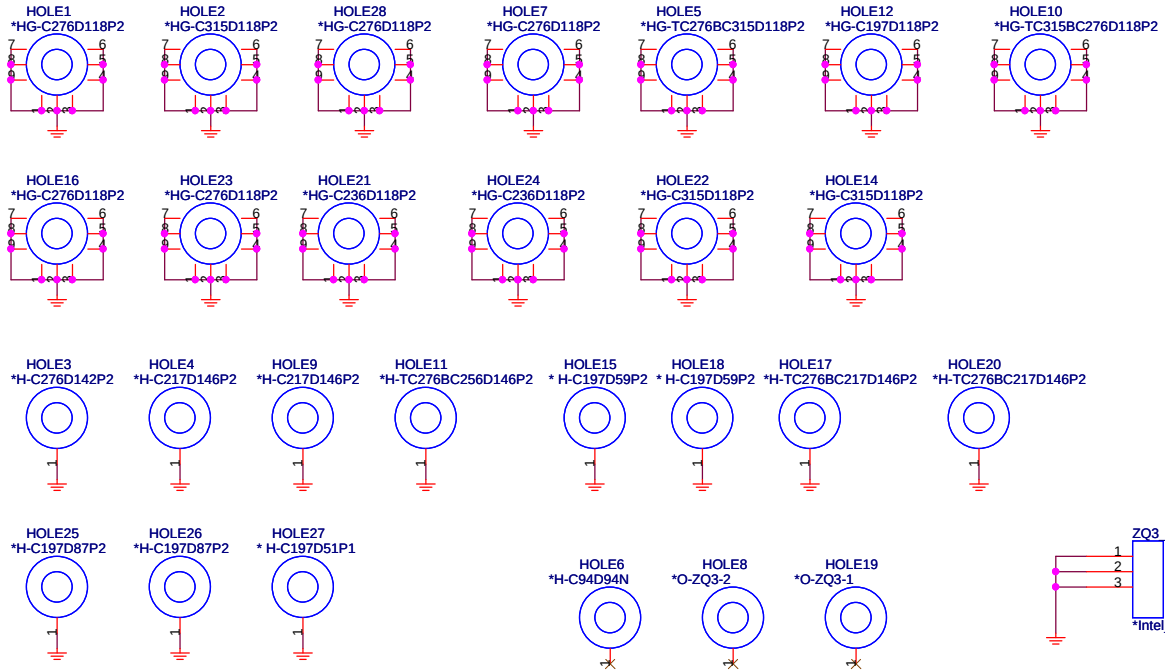
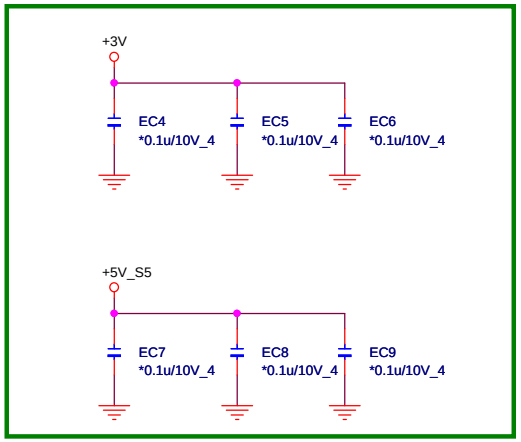
# INT K/B (KBC)




# TOUCHPAD & Finger-Printer CONN.(TPD)

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**PROJECT : ZQ3**

| Size | Document Number | Rev |
|---|---|---|
| | KB/TP+FP/CIR/BT/TPScreen | 1A |

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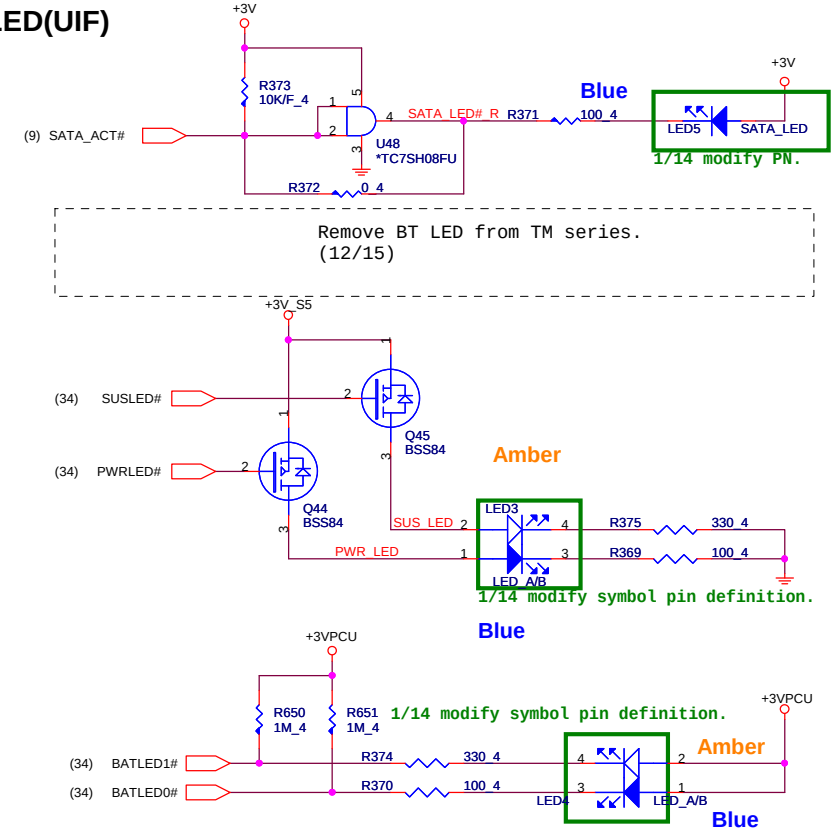
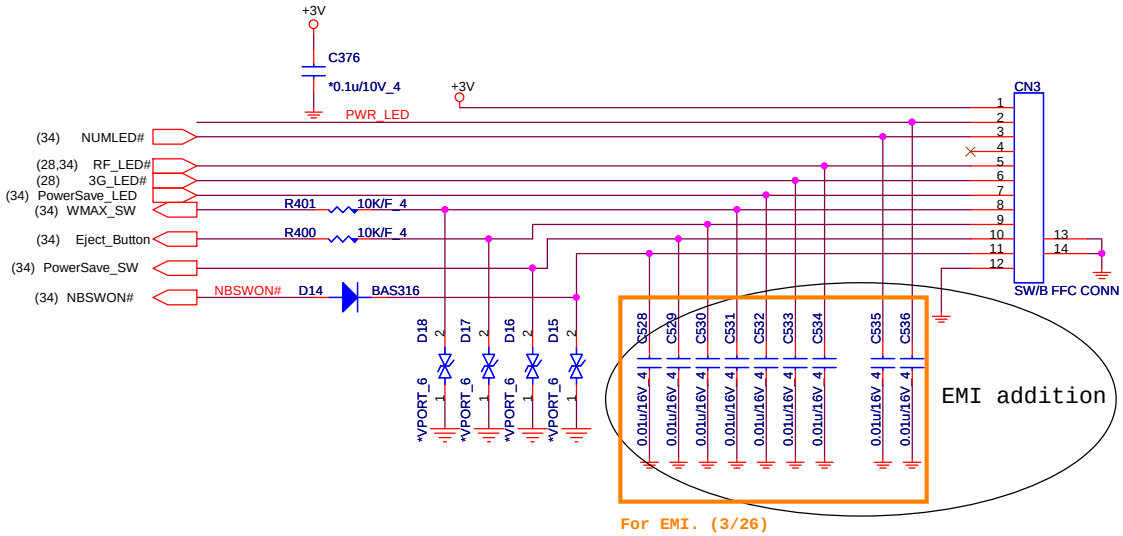
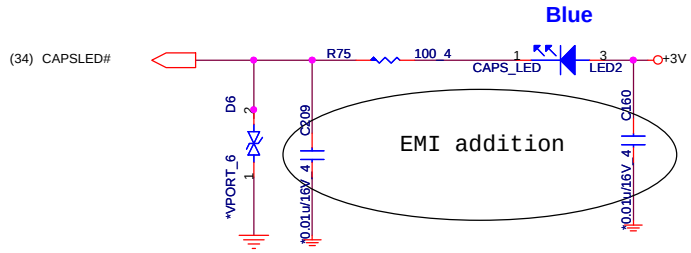
## M/B LED(UIF)

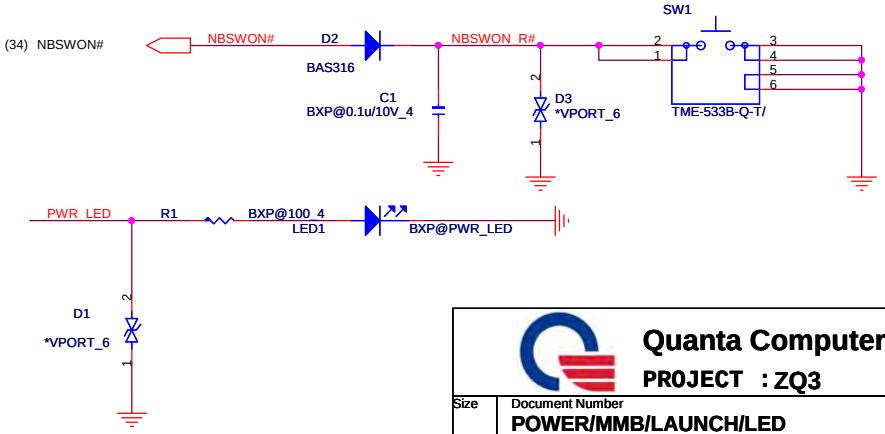



## SW BOARD CONNECTOR(UIF)




## M/B LED(UIF)




**Quanta Computer Inc.**

**PROJECT : ZQ3**

| Size | Document Number | Rev |
|---|---|---|
| | POWER/MMB/LAUNCH/LED | 1A |

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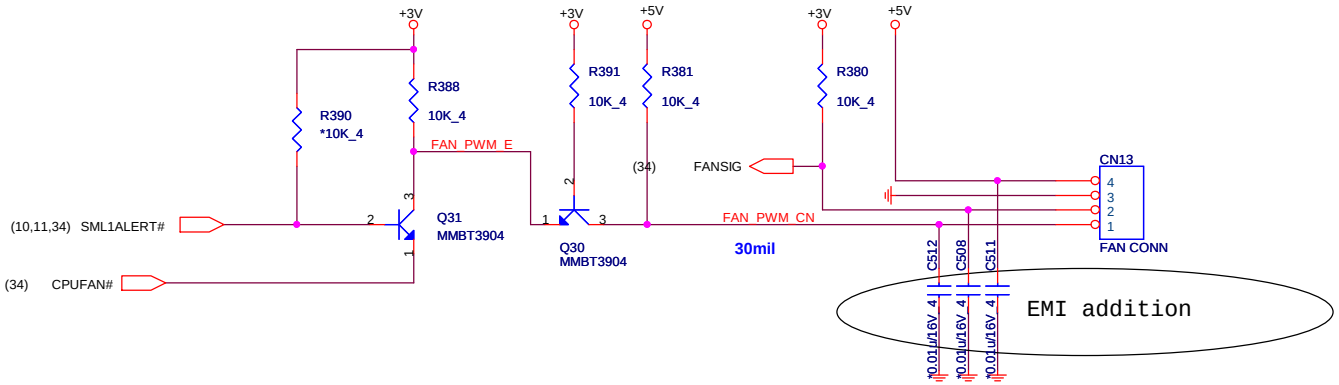
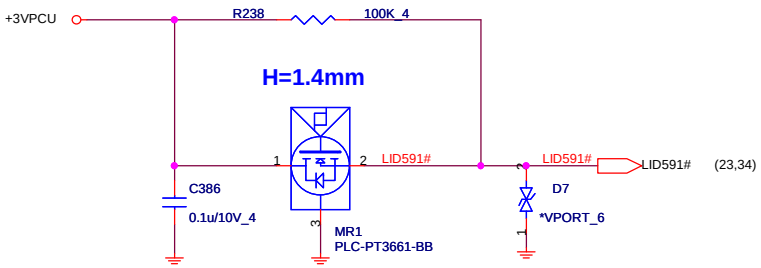
## CPU FAN(THM)




## HALL SENSOR(HSR)




Quanta Computer Inc.

PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | FAN/Thermal Protection | 1A |

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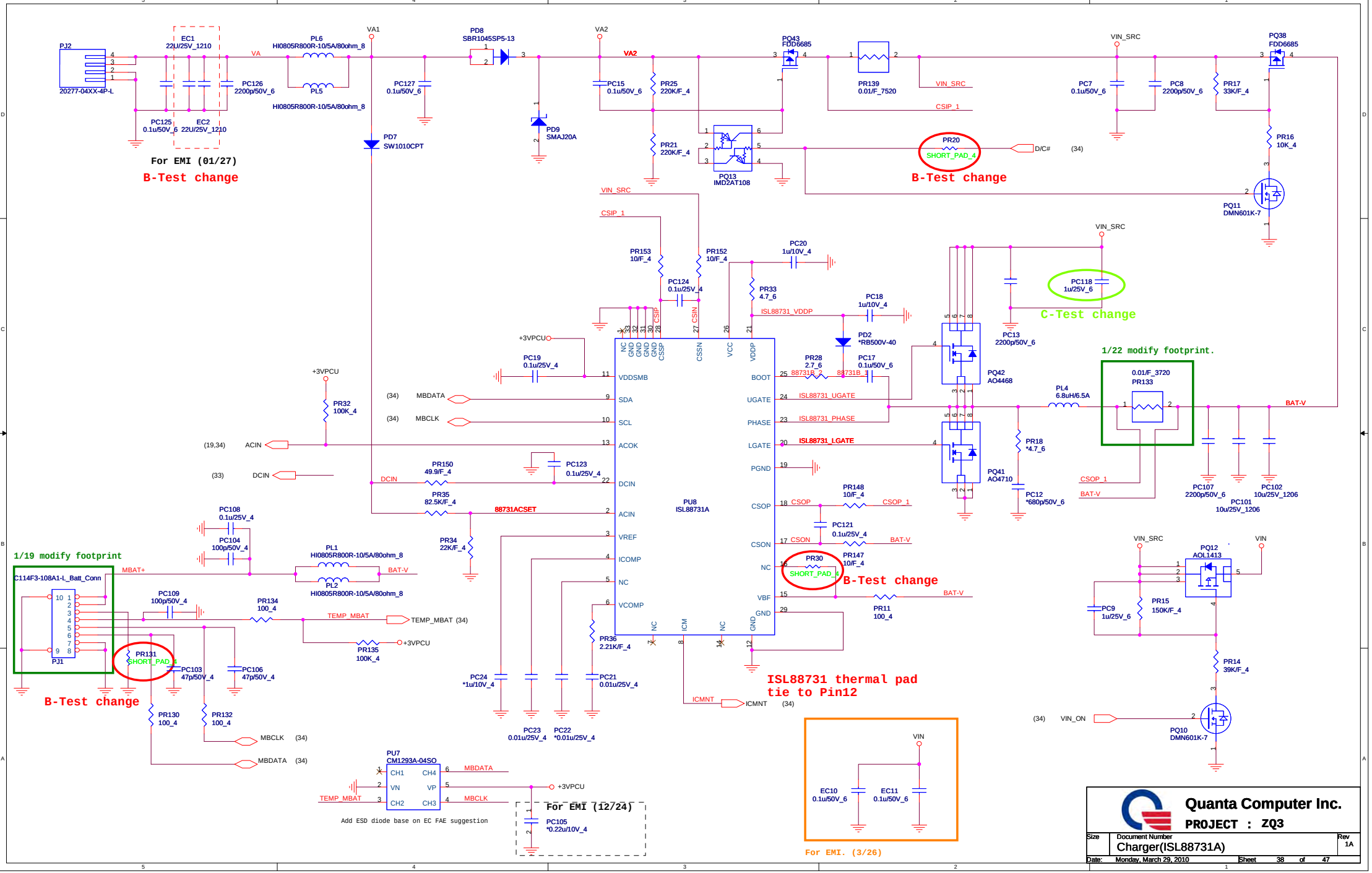


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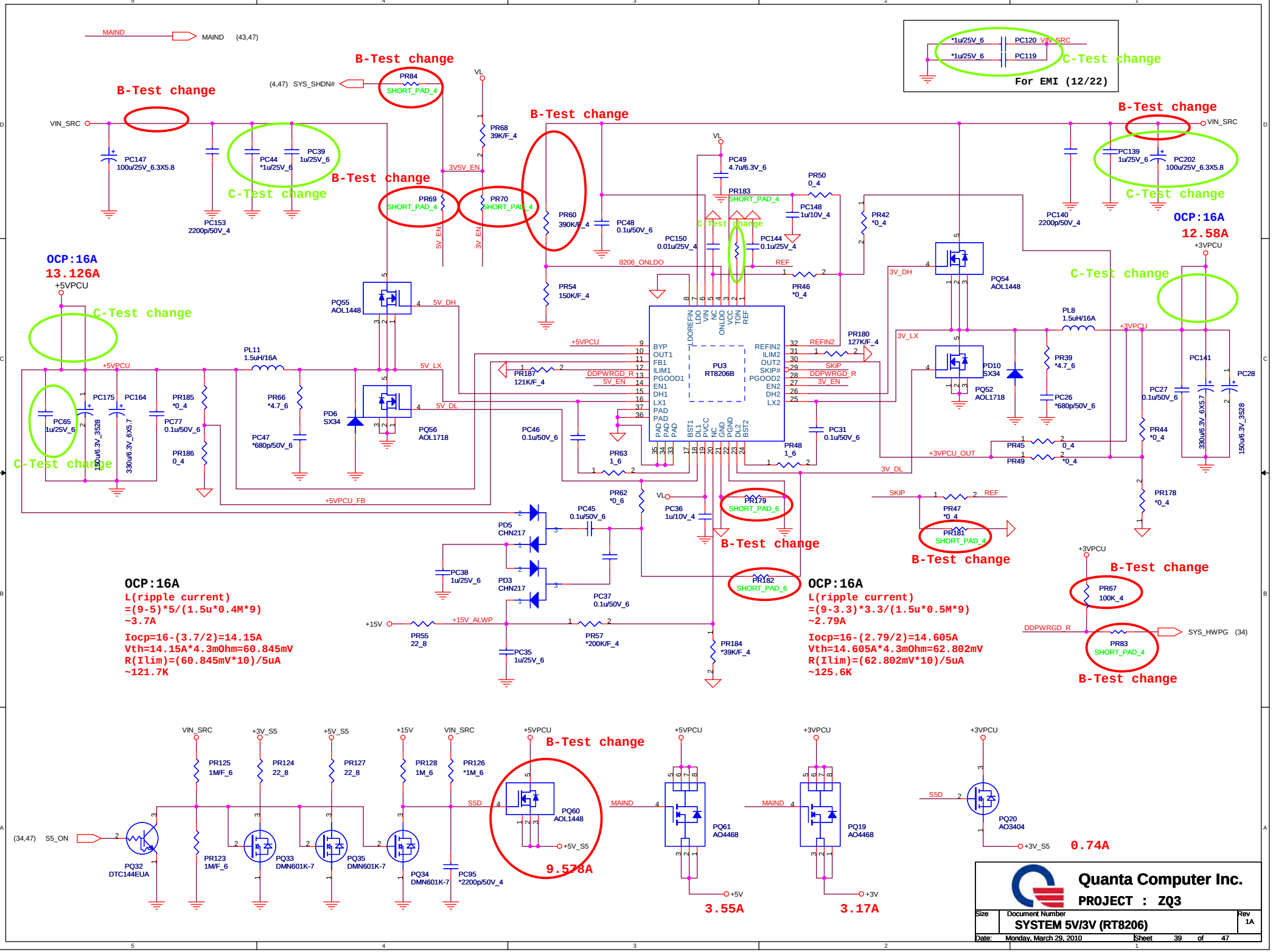
MAIND
MAIND (43,47)
B-Test change
(4,47) SYS_SHDN#
PR84
SHORT_PAD_4
VL
VIN_SRC
PC147
100u/25V_6.3X5.8
PC44
*1u/25V_6
PC39
1u/25V_6
C-Test change
PC153
2200p/50V_4
3V5V_EN
PR68
39K/F_4
PR69
SHORT_PAD_4
PR70
SHORT_PAD_4
5V_EN
3V_EN
PR60
390K/F_4
PC48
0.1u/50V_6
PC150
0.01u/25V_4
PC49
4.7u/6.3V_6
PR183
SHORT_PAD_4
PR50
0_4
PC148
1u/10V_4
PC144
0.1u/25V_4
PR42
*0_4
PC140
2200p/50V_4
PC139
1u/25V_6
PC202
100u/25V_6.3X5.8
OCP:16A
12.58A
+3VPCU
OCP:16A
13.126A
+5VPCU
8206_ONLDO
REF
PR46
*0_4
PR54
150K/F_4
PQ55
AOL1448
5V_DH
3V_DH
PQ54
AOL1448
PL8
1.5uH/16A
PL11
1.5uH/16A
5V_LX
3V_LX
PR180
127K/F_4
REFIN2
PR187
121K/F_4
DDPWRGD_R
5V_EN
SKIP
3V_EN
PU3
RT8206B
PD10
SX34
PQ52
AOL1718
PR39
*4.7_6
PC26
*680p/50V_6
PC141
PC28
PC27
0.1u/50V_6
PC65
1u/25V_6
PC175
PC164
PR185
*0_4
PC77
0.1u/50V_6
PR186
0_4
PR66
*4.7_6
PD6
SX34
5V_DL
PQ56
AOL1718
PC47
*680p/50V_6
PC46
0.1u/50V_6
PR63
1_6
PC31
0.1u/50V_6
PR48
1_6
PR45
0_4
PR49
*0_4
+3VPCU_OUT
3V_DL
PR44
*0_4
330u/6.3V_6X5.7
150u/6.3V_3528
330u/6.3V_6X5.7
+5VPCU_FB
PR62
*0_6
PC45
0.1u/50V_6
PC36
1u/10V_4
PR179
SHORT_PAD_6
PR178
*0_4
SKIP
REF
PR47
*0_4
PR181
SHORT_PAD_4
PD5
CHN217
PD3
CHN217
PC38
1u/25V_6
PC37
0.1u/50V_6
PR182
SHORT_PAD_6
OCP:16A
L(ripple current)
=(9-5)*5/(1.5u*0.4M*9)
~3.7A
Iocp=16-(3.7/2)=14.15A
Vth=14.15A*4.3mOhm=60.845mV
R(Ilim)=(60.845mV*10)/5uA
~121.7K
OCP:16A
L(ripple current)
=(9-3.3)*3.3/(1.5u*0.5M*9)
~2.79A
Iocp=16-(2.79/2)=14.605A
Vth=14.605A*4.3mOhm=62.802mV
R(Ilim)=(62.802mV*10)/5uA
~125.6K
+15V
PR55
22_8
+15V_ALWP
PR57
*200K/F_4
PC35
1u/25V_6
PR184
*39K/F_4
PR67
100K_4
DDPWRGD_R
PR83
SHORT_PAD_4
SYS_HWPG (34)
*1u/25V_6
PC120
VIN_SRC
PC119
For EMI (12/22)
PR125
1M/F_6
PR124
22_8
PR127
22_8
PR128
1M_6
PR126
*1M_6
+3V_S5
+5V_S5
+15V
S5D
(34,47) S5_ON
PQ32
DTC144EUA
PR123
1M/F_6
PQ33
DMN601K-7
PQ35
DMN601K-7
PQ34
DMN601K-7
PC95
*2200p/50V_4
PQ60
AOL1448
9.578A
MAIND
PQ61
AOL4468
+5V
3.55A
PQ19
AOL4468
+3V
3.17A
PQ20
AO3404
0.74A
Quanta Computer Inc.
PROJECT : ZQ3
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev
1A
Date: Monday, March 29, 2010
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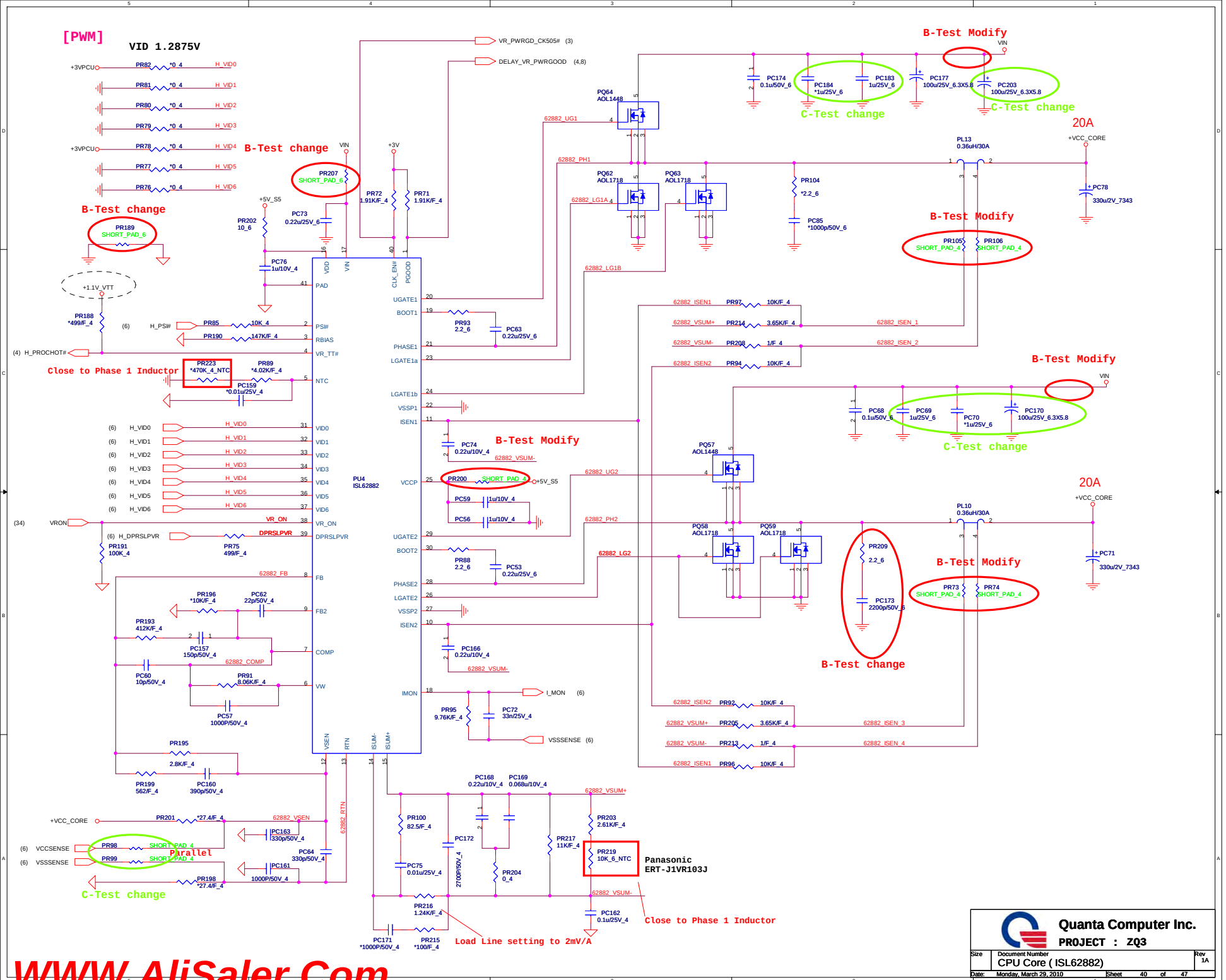


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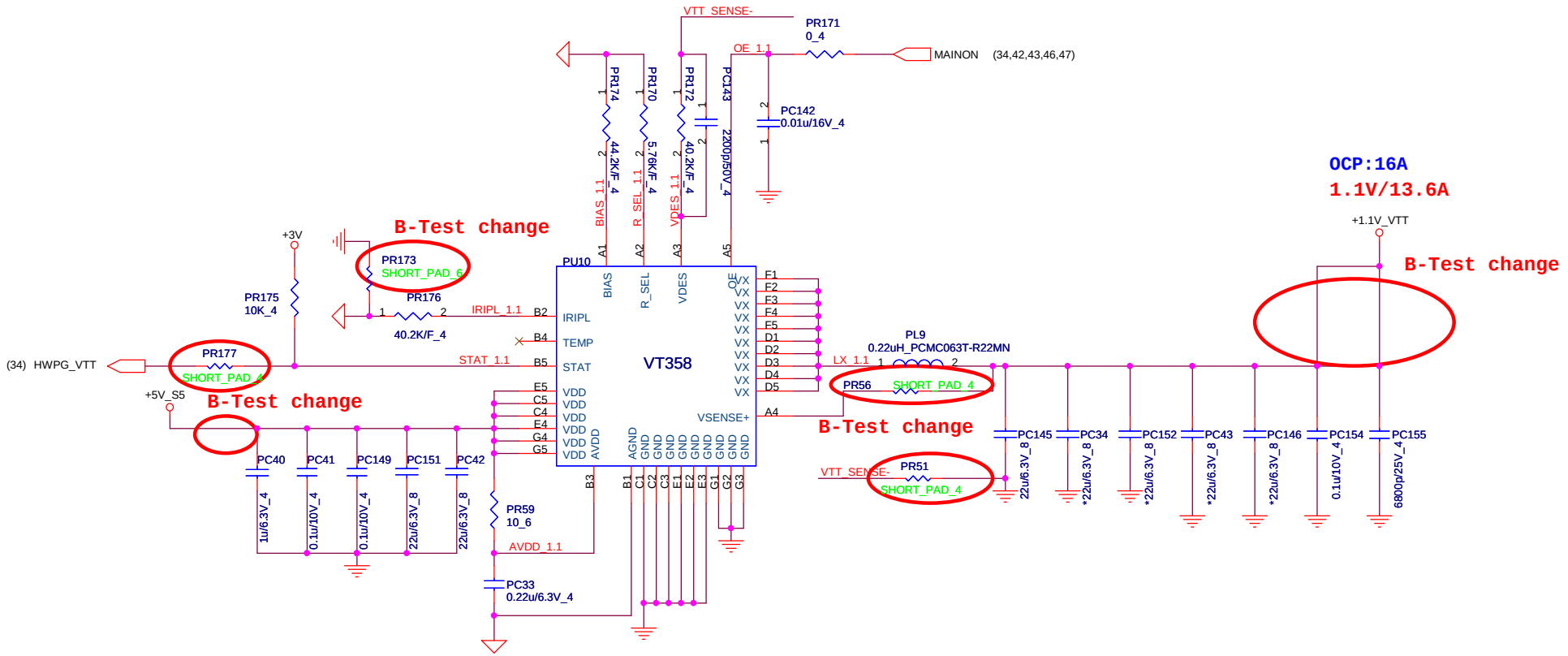
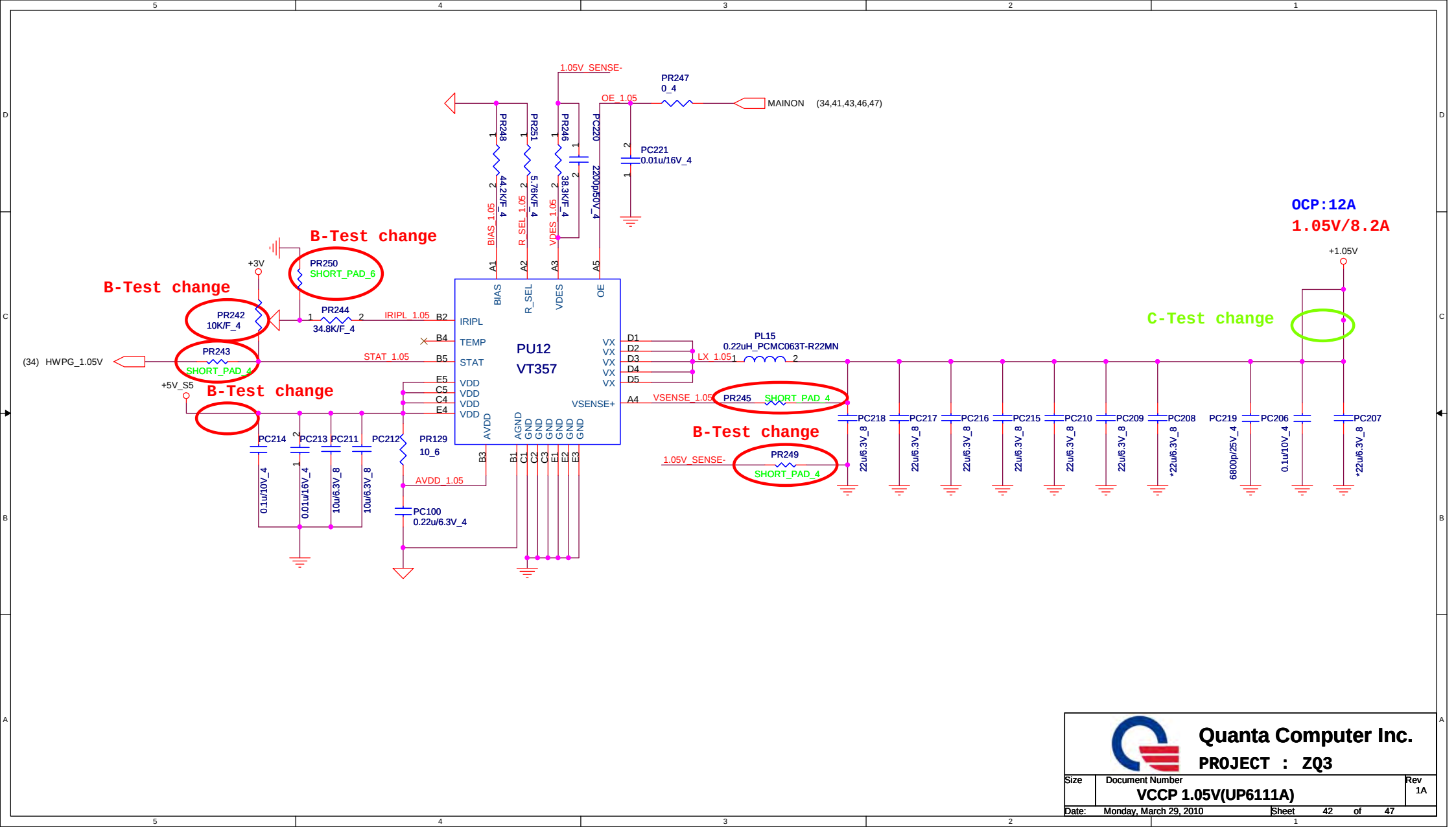
[PWM]




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZQ3 | | |
| Size | Document Number: +VTT (UP6111A) | Rev 1A |
| Date: Monday, March 29, 2010 | Sheet 41 of 47 | |




Quanta Computer Inc.

PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | VCCP 1.05V(UP6111A) | 1A |

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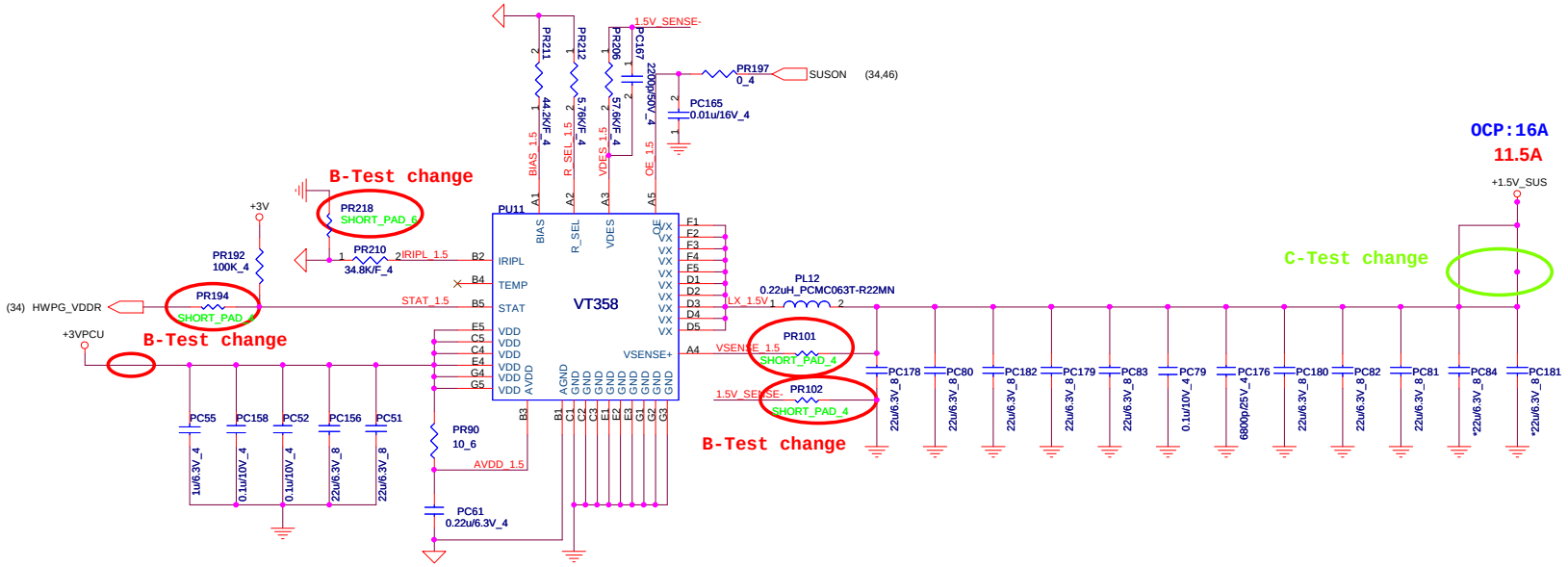
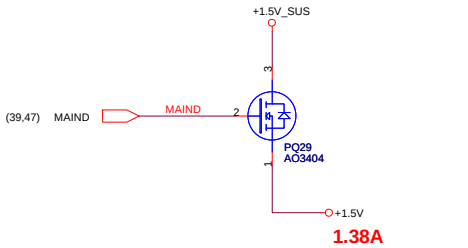
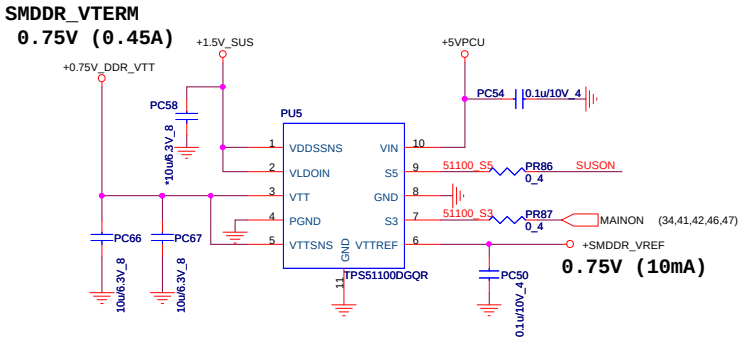
[PWM]



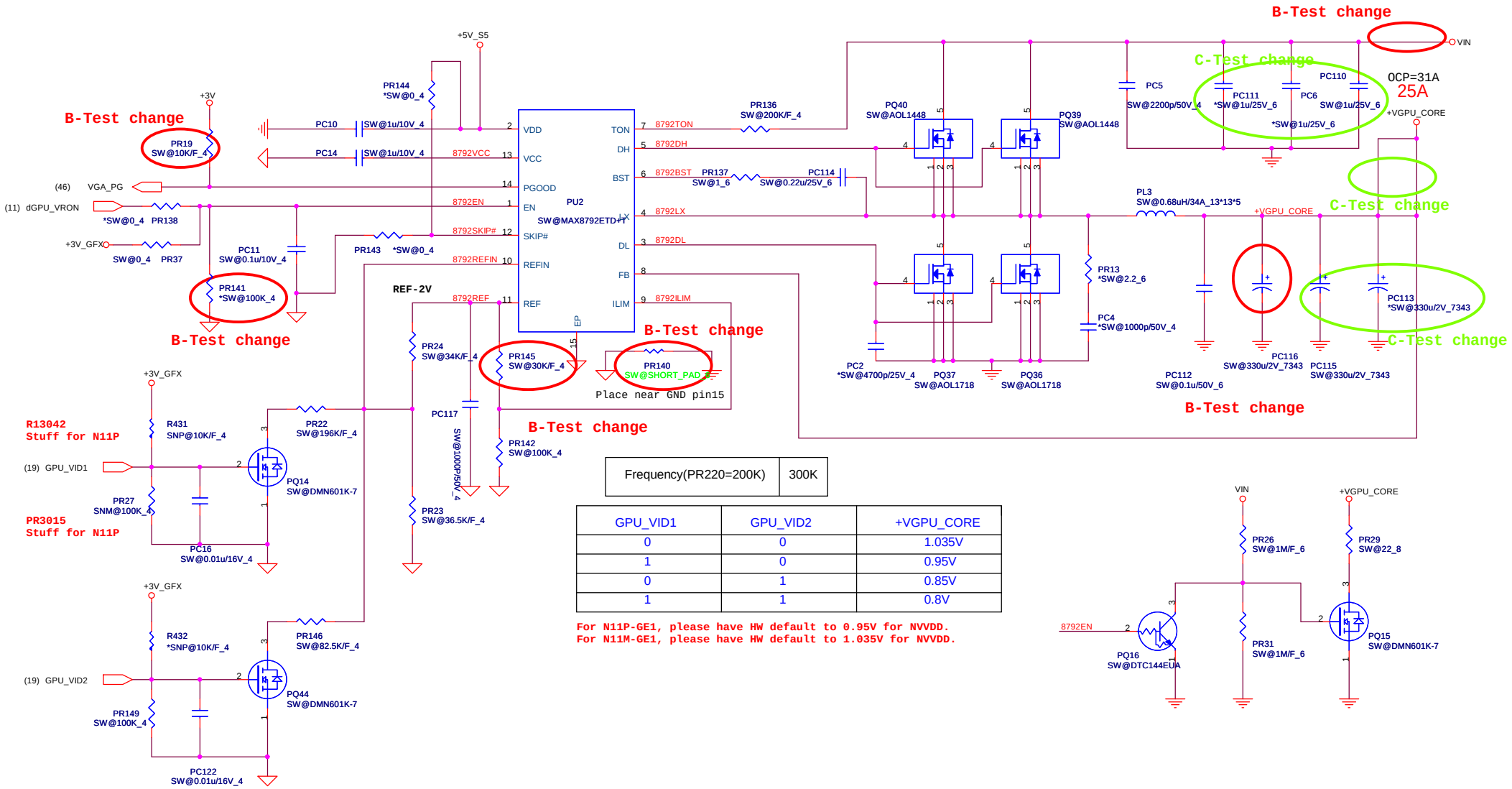

| | S3 | S5 | VTT | REF | +1.5VSUS |
|---|---|---|---|---|---|
| S0 | 1 | 1 | ON | ON | ON |
| S3 | 0 | 1 | ON | ON | OFF |
| S4/S5 | 0 | 0 | OFF | OFF | OFF |

Quanta Computer Inc.

PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | DDR 1.5V(TPS51116) | 1A |

Date: Monday, March 29, 2010 Sheet 43 of 47




| Frequency(PR220=200K) | 300K |
|---|---|

| GPU_VID1 | GPU_VID2 | +VGPU_CORE |
|---|---|---|
| 0 | 0 | 1.035V |
| 1 | 0 | 0.95V |
| 0 | 1 | 0.85V |
| 1 | 1 | 0.8V |

For N11P-GE1, please have HW default to 0.95V for NVVDD.
For N11M-GE1, please have HW default to 1.035V for NVVDD.

12/9 R13042,R13043 move to PWM IC circut page

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PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | GPU CORE(MAX8792) | 1A |

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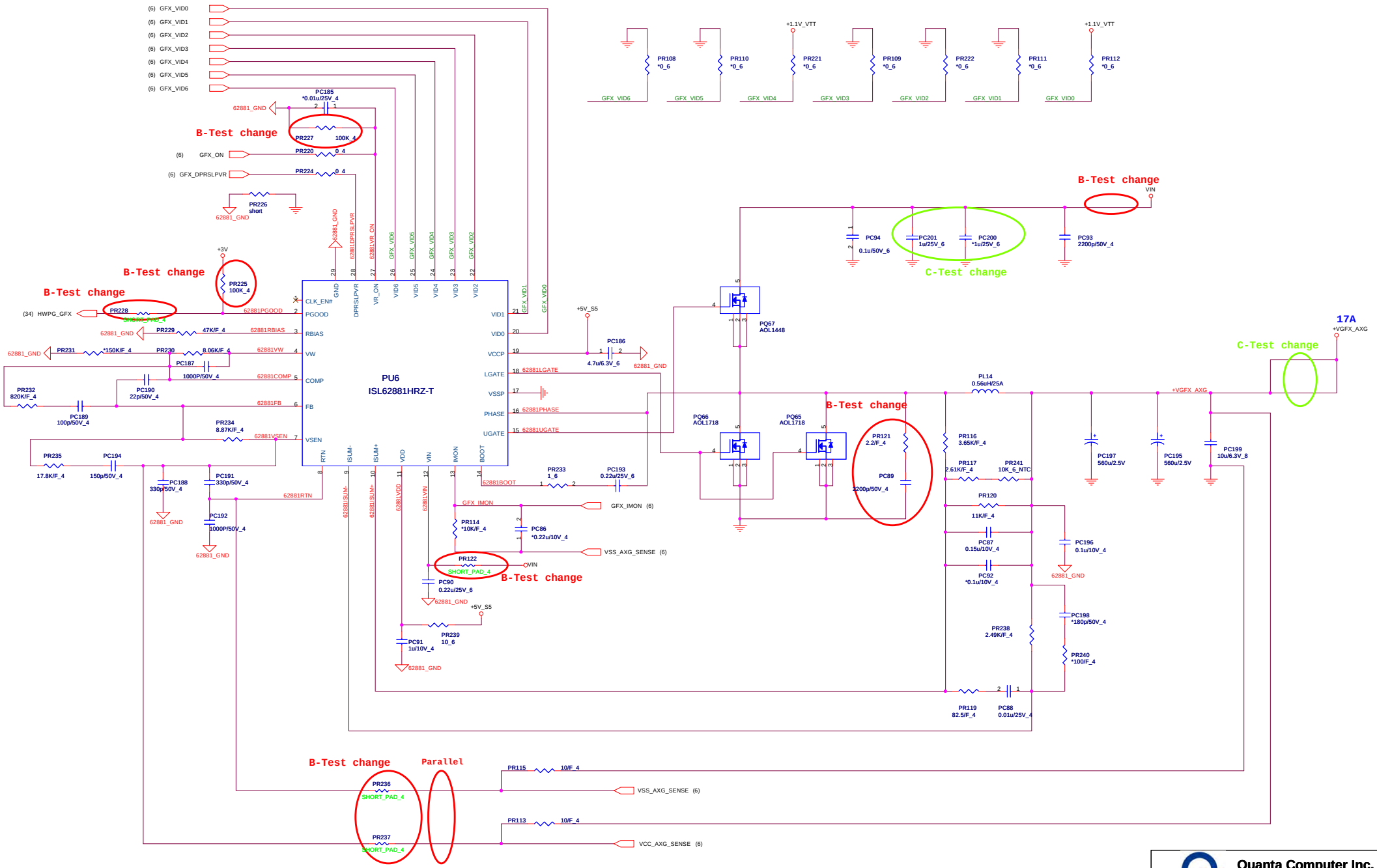
# Int_VGA [PWM]

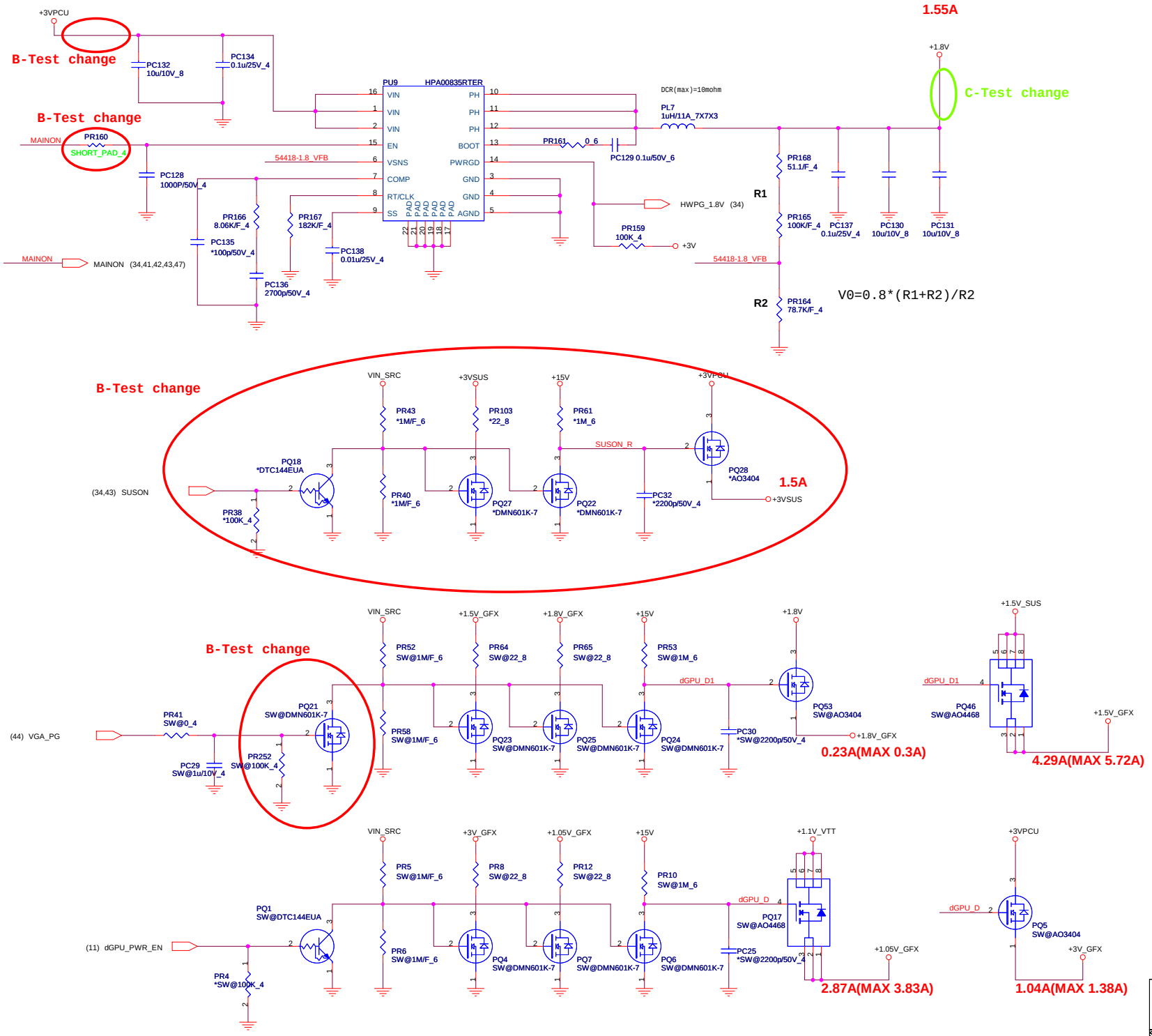



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | +VGFX_AXG (ISL62881) | 1A |

Date: Monday, March 29, 2010 Sheet 45 of 47

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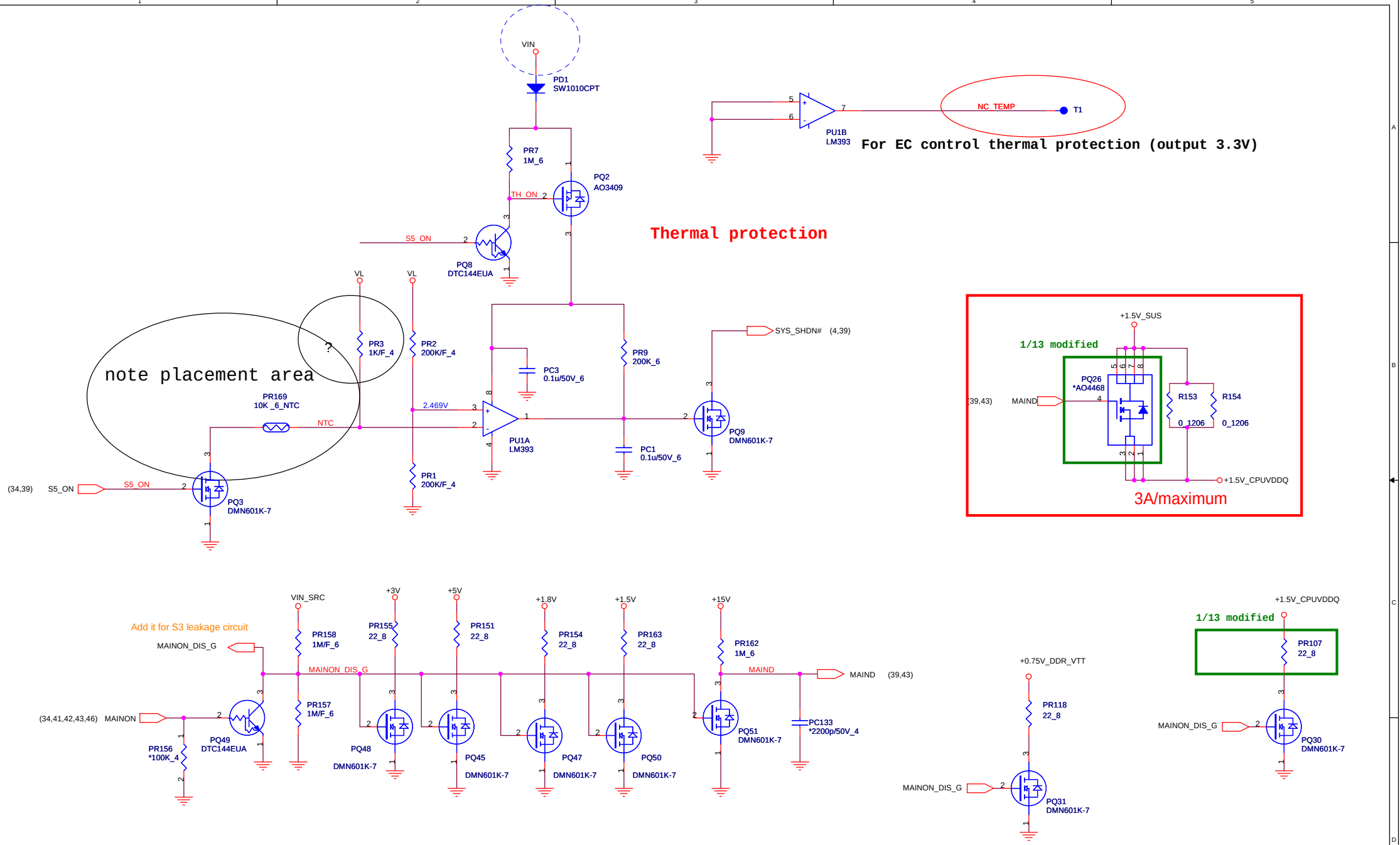
Quanta Computer Inc.

PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | (GPU_Power/1.8V) | 1A |

Date: Monday, March 29, 2010 Sheet 46 of 47




Quanta Computer Inc.

PROJECT : ZQ3

| Size | Document Number | Rev |
|---|---|---|
| | Thermal Protection | 1A |

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